ANNALS OF THE FACULTY OF ENGINEERING HUNEDOARA
2004, Tome II, Fascicole 2

DIGITAL INTERFACE BOARD WITH FOUR 8-BYTE OUTPUT PORTS

[1] TIRIAN Gelu Ovidiu

[1] University "POLITEHNICA" TIMISOARA,
Faculty of Engineering HUNEDOARA

Summary:

This work presents a digital interface board with four 8-byte output ports to be connected to the ISA bus of the computer. The 4 ports can be addressable anywhere in the address space of the port by using the 3 jumpers.

Key words: *digital interface, output ports.*

1. INTRODUCTION

The digital interface board with four 8-byte output ports has been created in didactic scope.

The output ports have a 25 mA stream capability (in either HIGH or LOW state). The four output ports are implemented by four 74373 circuits (8-byte Bus Driver with HZ and LATCH capability).

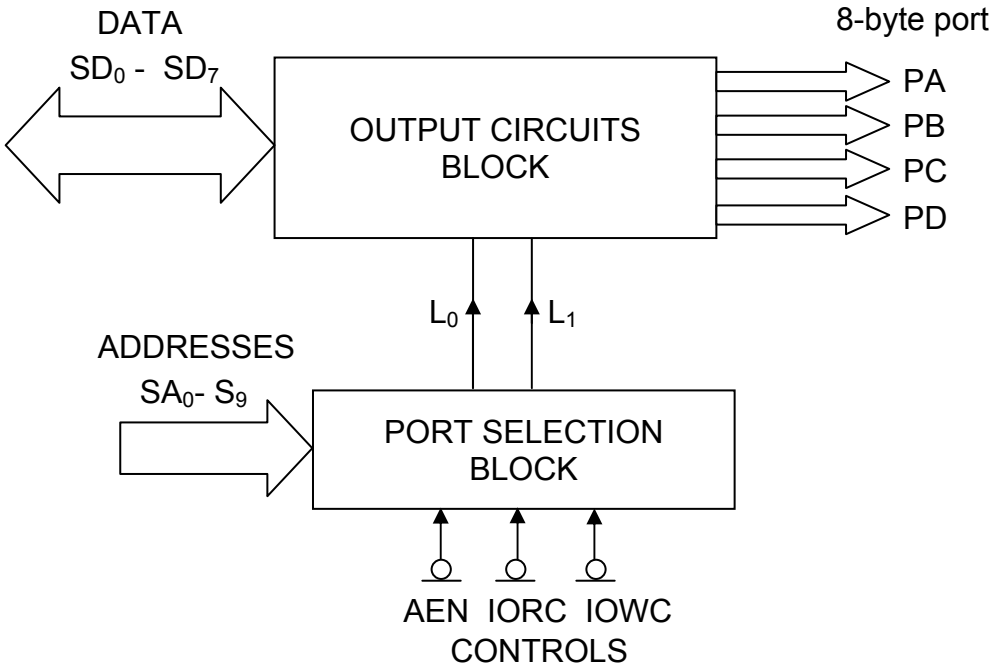

Fig. 1. *The block diagram*

The block diagram of the board is described in Fig. 1 and contains the selector block implemented by 4 BCD decimal decoders, as well as the input circuits block that has 4 output circuits.

These two blocks are connected to the address, data and control buses, as follows:

a) The input circuits block to the data buses (SD_0- SD_7)
b) The port selection block to the address buses (SA_0- SA_9) and to the control buses (AEN, IORC, IOWC).

2. THE SYNTHESIS OF THE DECODER

The decoders can be defined as demultiplexer circuits for which the input is at logic level 1 I= 1 (+V). In this case, according to the Boolean operation that describes the action of the DEMUX, the circuit becomes a code identifier. This is realized because each output will identify one of the input operations. Therefore, the decoders can be represented as a block diagram like in Fig. 2.

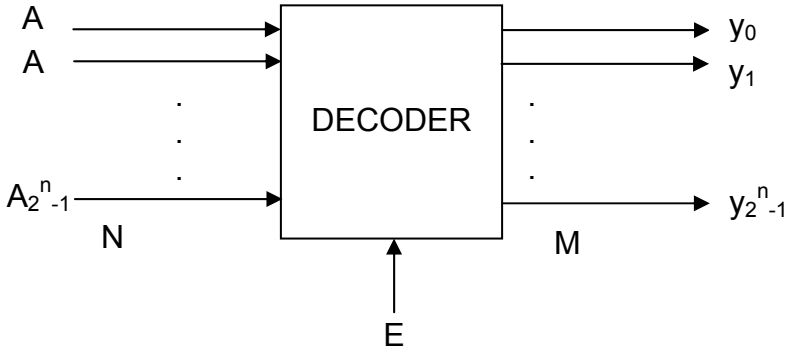

Fig. 2. *The block diagram*

Let N be the binary number expressed by the input combination and M the binary number expressed by the output combination. Thus, it can be written:

$$M= 2^N$$

As one can notice, the expression obtained is an inverse function of the function realized by the decoder, for which the encoding outputs were obtained as $M= \log_2 N$.

The decoders can also be found as an M.S.I. circuit, implemented in TTL (with the active outputs on 0) and CMOS (with the active outputs on 1) technology.

Generally, these integrate circuits are 4-byte decoders.

The binary-decimal decoder

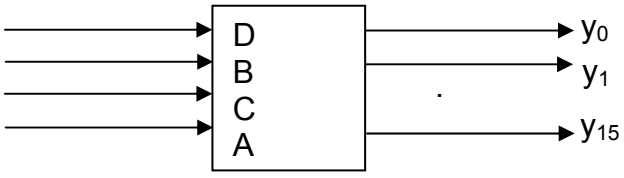

Fig. 3 *The block diagram*

Related to the principle of working, the decoders can be:

- binary
- BCD
- BCD- 7 segments

The working of the circuit can be briefly described in the truth table (Table 1):

Table 1

No.	D	C	B	A	Active outputs	Active outputs
0	0	0	0	0	y_0	y_0
1	0	0	0	1	y_1	y_1
2	0	0	1	0	y_2	y_2
3	0	0	1	1	y_3	y_3
4	0	1	0	0	y_4	y_4
5	0	1	0	1	y_5	y_5
6	0	1	1	0	y_6	y_6
7	0	1	1	1	y_7	y_7
8	1	0	0	0	y_8	y_8
9	1	0	0	1	y_9	y_9
10	1	0	1	0	y_{10}	-
11	1	0	1	1	y_{11}	-
12	1	1	0	0	y_{12}	-
13	1	1	0	1	y_{13}	-
14	1	1	1	0	y_{14}	-
15	1	1	1	1	y_{15}	-

The decoder can identify by its outputs any combination of inputs. The binary-decimal decoders can be used for the implementation of logical functions, but they can especially be found in the memory circuits, for the selection of the cells addressed at a certain time. They can also be used for the selection of the memory circuits and input-output circuits within the systems with μP.

The decoding was carried out by means of 4 decoders. The four binary-decimal decoders (ic1-ic4) achieve a complete decoding of the address space reserved to the ports, using the SA9-SA0 and AEN, IORC, IOWC signals (table 2).

Table 2

	SP1			SP2			SP3						
AEN	SA 9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IOWC	IORC	DESCRIPTION
1	X	X	X	X	X	X	X	X	X	X	X	X	-
0	X	X	X	X	X	X	X	X	X	X	X	X	-
										0	0	1	PA
										1	0	1	PB
										0	1	0	PC
										1	1	0	PD
										X	1	1	IMPOSSIBLE
	0 – 34			0 – Fh			0 - Fh						

In order to assign the port addresses, 340h- 341h for example, the JP1- JP3 jumpers must be set as it follows:

JP1	JP2	JP3
X ⟶ 6	Y ⟶ 3	Z ⟶ 0

3. CONCLUSIONS

This work carried out the study of the board that will be connected to the ISA bus of the computer. This board was built and its functioning was tested by means of a program that represents a four non-multiplexed display-cell decimal counter.

4. REFERENCES

1. *Poantă, A., Sisteme cu microprocesor, Note de curs*
2. *Lupu Stăncescu, Microprocesoare. Circuite. Proiectare, Editura Militară, Bucureşti, 1986*