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DESIGN AND CREATION OF A DEVICE MEANT TO MEASURE THE LEVEL OF LIQUID

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ABSTRACT:
The paper presents system for measurement fluid level between 0÷50 cm with a good precision. The system could be used on the industrial processing's and industrial automation labs.

KEY WORDS: level transducer, analogue /digital converter, DDD

1. GENERALITIES

The level of a liquid or the interface level between to liquids can be determined by monitoring the separation surface between them, by measuring the hydrostatic pressure exerted by the liquid column, or by indirect methods. In the paper, the level of the liquid level is measured by means of a level transducer based on level measuring with a floater.

2. THE BLOCK DIAGRAM OF THE LEVEL MEASURING DEVICE

The block diagram of the level measuring device is given in figure 1 and consists in:

- level transducer(LT);
- analogue /digital converter (A/D C);
- decimal display device (DDD).

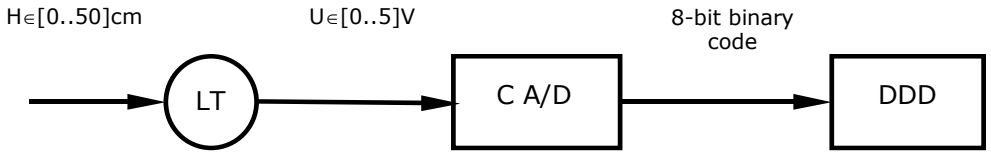

Fig. 1 *The block diagram of the level measuring device.*

Level $H \in [0..50]$ *cm* is converted by transducer LT, into voltage $U \in [0…5]$ *V*.
The analogue/digital converter A/D C converts voltage *U* into 8-bit binary code.
The decimal display device DDD has two roles:

- The read and interpret the binary code read;
- To display the measured inflow.

3. THE DESIGN OF THE COMPONENT BLOCKS

We chose a transducer based on level measuring by means of a floater.
The characteristics of the level transducer:

- domain: 0…50*cm*;
- output: 0…5*V* c.c.;
- source: 12*V*.

We used an 8-bit analogue /digital converter with 4 multiplex inputs. These inputs can be configured for the following means of operation:

- to read one input only (measures the voltage between the input and the null);
- differential reading (measuring the voltage between two inputs)

The converter turns the input voltage corresponding to one of the operation means, into an 8-bit binary number, the inputs to be read being programmed by the user.

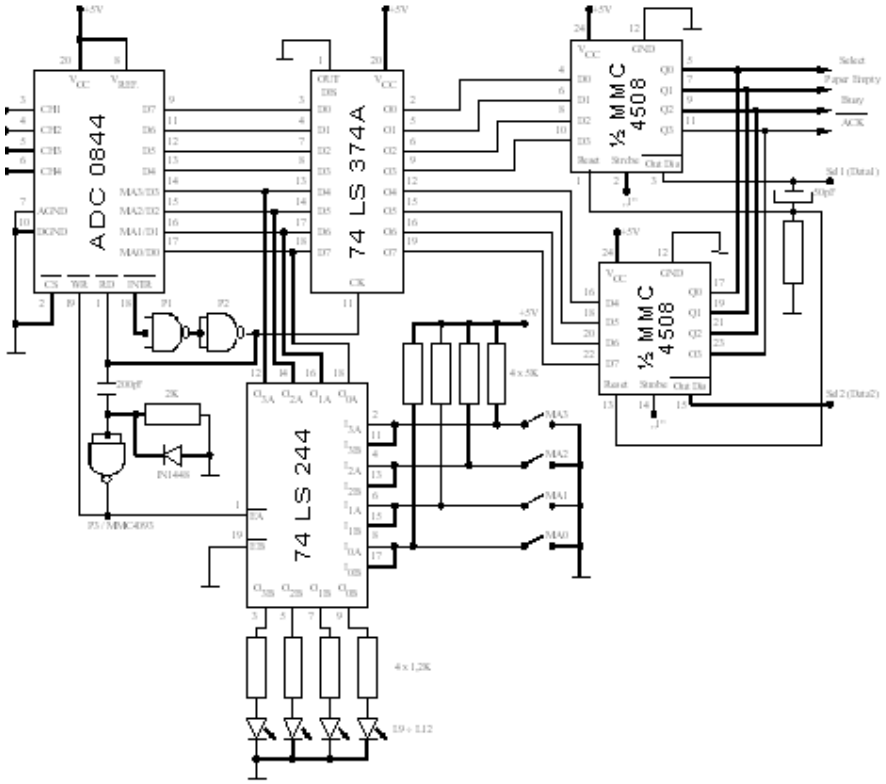

Fig. 2. Diagram of the analogue / digital converter

Circuit ADC0844 is a CMOS analogue /digital converter with successive, 8-bit approximations and with multiplex analogue inputs. It contains an internal clock and a logic control unit which, according to the command that was given, i.e. reading (on $\overline{RD}$ pin) or writing (on $\overline{WR}$ pin), generates the binary code corresponding to the voltage converted to pins D0÷D7 in order to be read, respectively switches to high impedance the binary outputs and reads from pins MA0÷MA3 the code set by the user, code that triggers the multiplexor at the input of the integrated circuit.

The conversion time set by the internal clock is 40μs.

During the writing command, circuit 74LS244 (which contains 8 non-reverse separators – buffers with 3-STATE outputs) reads the binary code corresponding to the 4 switches MA0÷MA3, code that generates inputs MA0÷MA3 of I.C. ADC0844. This code is shown by LED's L9÷L12.

During the reading command, circuit ADC0844 generates at outputs D0÷D7 the binary code corresponding to the converted voltage, which is read by circuit 74LS374A (circuit containing 8 LATCH-D type bistables with 3-STATE outputs) and is displayed by e LED's L1÷L8.

The reading and writing commands are obtained from the signal generated by I.C. ADC0844 at pin $\overline{INTR}$, signal corresponding to the end of conversion.

Port P3 together with the corresponding passive components make up a mono-stable (a delay circuit) that creates the writing impulse, delaying it with respect to the reading impulse, by the necessary time, so that I.C. 74LS374A can memorize the 8-bit binary code after which, this signal triggers the writing of the 4-bit code in the internal LATCH of ADC0844.

For the case of one input (reading with respect to the null) relation:

$$N = \frac{V_i}{\frac{V_{REF.}}{2^8 - 1}} = V_i \cdot \frac{255}{V_{REF.}} \quad (1)$$

is being checked, where:
N - the decimal number corresponding to the binary code read;
$V_{REF.}$ - the reference voltage (+5V);
V_i is - the input voltage.

When reading is being made differentially (between two inputs), relation:

$$N = \frac{V_d}{\frac{V_{REF.}}{2^8 - 1}} = V_d \cdot \frac{255}{V_{REF.}} \quad (2)$$

is being checked, where:
N - the decimal number corresponding to the binary code read;
$V_d=V_i-V_j$ - the difference between the voltages corresponding to the two inputs;
$V_{REF.}$ - the reference voltage (+5*V*);

The resulting code does not depend on the input voltages and the null, but on the difference between the two voltages. Switches MA0÷MA3, are set according to one of the codes given in the table below, table that characterizes the multiplexing function of the analogue / digital converter.

The integrated circuit MMC4508 contains two identical 4-bit latches with pins STROBE, RESET and $\overline{OUTPUT\quad DISABLE}$ separately.

With line STROBE in high state the data on inputs D correspond to the outputs Q on condition line DISABLE be in low state. Changing line STROBE in low state, the data are blocked in the latch. One high on RESET forces the outputs to a low level with respect to the state of STROBE inputs. The outputs are forced to a state of high impedance for the applications on the bus by the DISABLE outputs, at a high level.

Characteristics:

- 2 independent 4-bit latches;
- 3 state outputs;
- mean work rates: $T_{plh}=T_{pll}=70ns$ at $V_{dd}=10V$ and $C_l=50pF$.

No.	Code binary				Listen entries
	MA3	MA2	MA1	MA0	
0	0	0	0	0	1-2
1	0	0	0	1	2-1
2	0	0	1	0	3-4
3	0	0	1	1	4-3
4	0	1	0	0	1
5	0	1	0	1	2
6	0	1	1	0	3
7	0	1	1	1	4
8	1	0	0	0	1-2
9	1	0	0	1	2-1
10	1	0	1	0	3-4
11	1	0	1	1	4-3
12	1	1	0	0	4-1
13	1	1	0	1	4-2
14	1	1	1	0	4-3
15	1	1	1	1	P

The table of truth for the functioning of circuit MMC4508 is the following:

RESET	DISABLE	STROBE	D INPUT	Q INPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	Latched
1	0	X	X	0
x	1	X	X	Z

4. CONCLUSIONS

The device we created measures the liquid level between 0…50 cm ensuring a high precision of the measurements. It is being used for different measurements during the laboratory classes of Industrial Automation, but also in industrial processes.

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