JOURNAL OF ENGINEERING annals OF FACULTY OF ENGINEERING HUNEDOARA

FABRICATION PROCESS OF SILICON-ON-INSULATOR AND LATER BIPOLAR TRANSISTORS

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ABSTRACT
Silicon on Insulator (SOI) has long been the forerunner of the CMOS technology in the last decade offering superior CMOS with higher speed, higher density, and excellent radiation hardness and reduced second order effects for submicron VLSI applications. The traditional SOI structure consists of a silicon dioxide layer sandwiched between a top thin silicon layer in which devices are built and the silicon substrate. Silicon-On-Insulator materials differ from normal bulk in that an insulating layer is present underneath the active device layer. The formation of a device quality single crystal silicon layer on top of the insulator is not a simple task. Over the years, various methods have been developed and they are briefly described in this paper. However, the purpose of this paper is to review the fabrication process of bipolar junction transistors (BJT) on thin film Silicon on Insulator (TFSOI) wafer. As results, it can be concluded that fabricating, the base, emitter and collector regions of bipolar transistors will be accessible at the top surface of thin film silicon on insulator substrate. Additionally, fabrication bipolar junction transistors by using planar process easier to be made inside laboratory's school of physics USM.
Keywords:
Silicon-On-Insulator (SOI), Thin film silicon on insulator (TFSOI), Bipolar junction transistors (BJTs).

1. INTRODUCTION

A basic SOI structure consists of a thin Silicon film over an insulating layer on top of a bulk Silicon substrate as shown in Figure (1). The top Silicon layer is used for active devices while the bottom bulk Silicon substrate acts as a mechanical support. Because the sandwiched insulating film is normally Silicon dioxide, it is also known as buried oxide (BOX). Other types of buried dielectric films have been considered and will be discussed in a later section. Some prominent advantages of SOI active circuit elements include radiation hardness, high-temperature operation, reduced junction capacitance(giving faster speed) eliminated circuit latch-up, and low power consumption (low voltage power supplies) for scaled devices (El-Kareh *et al.*, 1995; Colinge *et al.*, 1991; Hurley *et al.*,1995; Colinge, 1995; Colinge, 1994). Thought, the aforementioned features are in general motivation for SOI structures to be explored, manufacturability and cost must further merit the SOI technology (El-Kareh *et al.*, 1995; Nowak *et al.*, 1994; Hosack, 1993; Brady and Haddad,1993; Hwang 1993). The most commonly used thin-film SOI techniques to prepare SOI wafer are: SIMOX (separation by implantation of oxygen), BESOI (wafer bond and etch-back), and BSOI with "smart-cut" separation, and ZMR (zone melt re-crystallization). Both SIMOX and BESOI wafers are commercially available. SIMOX wafers are sold by IBIS technology in USA and by SOITECH in France, while BESOI wafers are sold by Hughes Danbury optical systems (Hosack, 1993). The smart-cut technology has yet to reach major commercial applications.

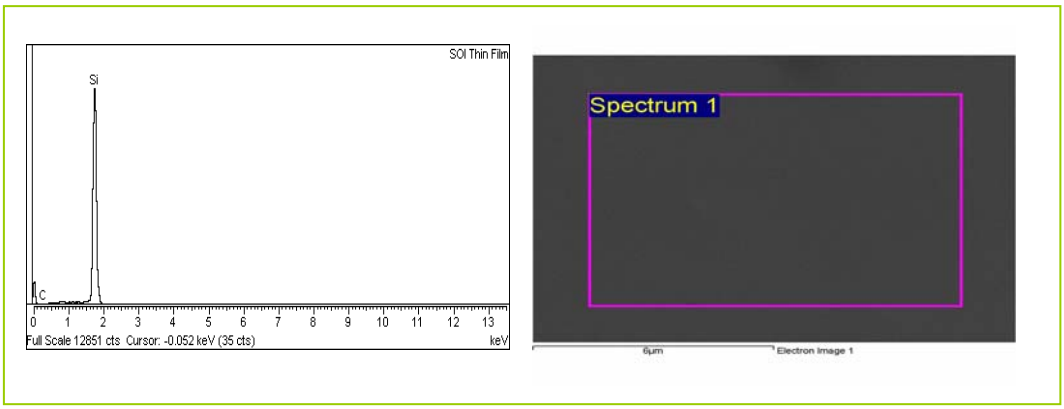

Figure 1. EDX Picture of Thin Film SOI

Another SOI technique is device islands of SOI by the use of SEG/ELO (selective epitaxial growth/epitaxial lateral overgrowth) (Neudeck *et al.*, 1997). Much like the improvements made to bulk Silicon material over the decades, SOI films must also reach the same, if not batter, material quality than that of bulk Silicon. Hence, important factors to SOI films are film quality, defect density, final film thickness, and thickness control (El-Kareh *et al.*, 1995). These factors will be addressed in the next two sections for, SEG/ELO SOI and Zone Melting Recrystallization (ZMR) techniques.

2. SOI by using SEG and ELO

Epitaxial growth of silicon can be blanket, such as in some standard CMOS and bipolar processes, or selective. In a selective epitaxial growth of silicon (SEG), single crystalline growth occurs in "seed" windows while little or no nucleation occurs on the oxide islands. Figure (2-a) shows the process steps to SEG growth. Silicon dioxide is an excellent dielectric material for both masking and insulation. If SEG continues to beyond the thickness of the oxide mask, the silicon epitaxy will self-seed and continue to grow laterally over the oxide regions as well as vertically. Hence, the structure of growth becomes ELO (epitaxial lateral overgrowth) as shown in figure (2-b). SEG/ELO is grown at 800^0- 1000^0C in 40-150 Torr CVD reactor and has an average growth rate of 0.1-0.25µm/min (Friedrich and Neudeck, 1989; Neudeck, 1990). The chemical gases normally employed include SiH_2Cl_2, HCl, and H_2. SiH_2Cl_2 and HCl mostly determine epitaxial growth rate. Because deposition of Silicon epitaxy must occurs at the growth front while etching/removal of nucleation on the oxide islands occurs, nominal ratio of lateral growth rate to vertical growth rate is approximately one. Immediately, one can see that the ELO structure resembles an SOI structure (Neudeck, 1990). Unlike SIMOX and BESOI mentioned above, an ELO structure is selective to regions needing SOI films. This provides maximum flexibility in using the best combination of bulk devices in the SEG and SOI devices in the ELO-SOI regions. This is especially true for 3-D devices (Friedrich and Neudeck, 1989; Neudeck, 1990; Glenn *et al.*, 1992a) as they noted that the ELO-SOI structure is not completely isolated from the bulk substrate because of the SEG as shown in figure (2-b). Therefore, a fully planarized method was developed to create a completely isolated ELO-SOI structure, from the substrate as well as from adjacent SEG regions (Glenn *et al.*, 1992a; Glenn *et al.*, 1992b). Figure (3-c) illustrates completely isolated SOI islands using SEG/ELO. Basically, selected SOI active regions are formed from multiple oxidation and oxide etch, and then SEG is allowed to overgrow until the ELO film the SOI active regions. Using the thick oxide as an etch-stop, excess ELO is chemical-mechanical polished (CMP) (Fury, 1995). Because the epitaxy is growth over the oxide surfaces, the SOI active region thickness is pre-defined by the thickness of two oxide growths. Thus, thin film SOI islands are possible as long as the CMP process tightly controls the surface defects. Defect density in the SOI islands generated from SEG/ELO growth has been observed to be below 300/cm2 (Kessler *et al.*, 1995; Neudeck, 1997). However, epitaxy quality is not the only concern in SEG/ELO growth. In addition, the interface between SEG and the surrounding oxide (Bashir *et al.*, 1995) and the degradation of oxide in SEG ambient (Friedrich &

Neudeck, 1989; Neudeck, 1990; Bashir *et al.*, 1995) are important to prevent any current leakage path at epitaxy/SiO2 interfaces in active regions. SEG sidewall defects have been investigated to be mainly due to the mismatch of the thermal expansion of oxide to the SEG, which can be improved (Bashir *et al.*, 1995). However, nitridation of oxides has recently been found to reduce both the SEG sidewall defects (Sherman, 1995) as well as resistance to oxide degradation in the SEG ambient (Fultz & Neudeck, 1995).

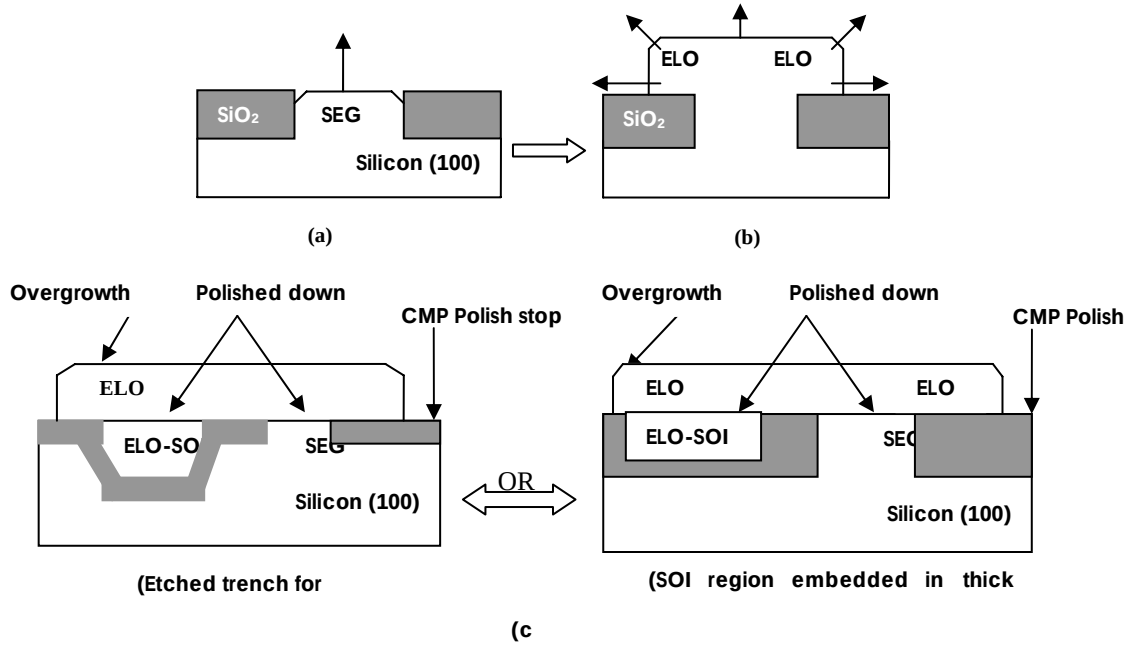

Figure 2. Ccross sections of (a) SEG growth, (b) ELO growth, and (c) SEG/ELO with CMP planarization forming completely isolated SOI "well".

3. ZONE MELTING RECRYSTALLIZATION (ZMR)

ZMR technology produces SOI structure by recrystallization of polysilicon film, deposited on oxidized silicon wafers as shown in figure (3). In the ZMR process thermal oxide (1-2lm thick) is first grown on a bulk-silicon substrate, followed by deposition of LPCVD amorphous or polycrystalline silicon film (0.5-1.0 lm thick) on the thermal oxide.

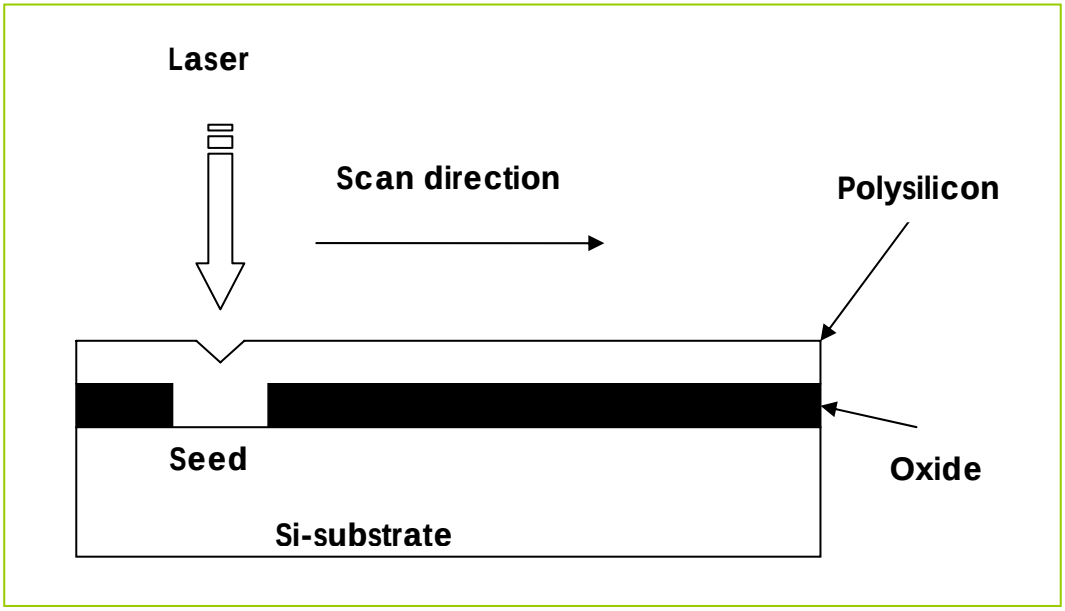

Figure 3. Process flows for Zone –Melting and Recrystallization

The whole structure is capped with a 2 lm thick layer of deposited thermal oxide covered by a thin nitride (Si_3N_4) layer. A molting zone, created by lamp, a graphite strip heater, an electron beam, or a laser, is scanned across the entire Silicon wafer. As a result, full liquid-phase recrystallization of Silicon wafer can be carried out in a single pass. Optimization parameters are the thickness of the oxide, Si film and capping layer, scanning speed and direction, seed interdistance, and heating power. Several stages are identified by increasing the heating which are as follows:

1) Silicon melting over oxide
2) Melting of silicon film at temperature at the top of the seed
3) Substrate melting underneath the seed
4) Substrate overheating below oxide;

The advantages of the ZMR process are the production of 3D integrated circuit that includes multifunctional operation, facilitation of parallel processing, optical sensing functions, and high speed.

4. FABRICATION PROCESSES

The planar process is made possible due to the fact that silicon dioxide (SiO_2) may be grown on the silicon substrate and then selectively removed from designated areas through photolithographic and etching techniques. The oxide effectively keeps any doping impurities from diffusing into the areas it covers and thus permits the formation of P or N regions over well defined areas on the substrate's surface. The oxide also serves to protect the junctions where they reach the surface of the sample from the surface contamination and it also isolates the three contacts from each other. Silicon dioxide (SiO_2) is excellent insulator.

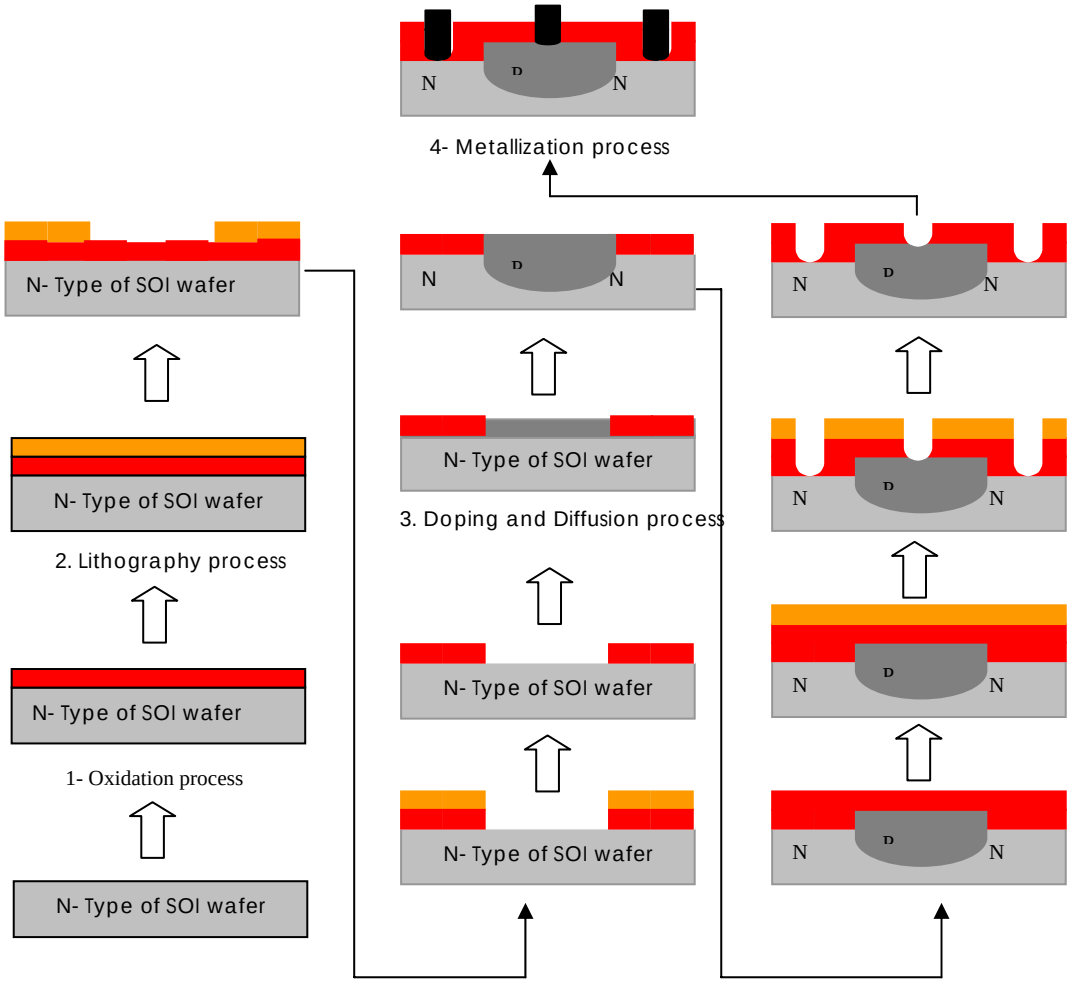

Figure 4. Subsequent of the steps fabrication process

Figure (4) shows the process steps required for the formation of a diffused SOI bipolar junction transistor. Theses are the steps that will be followed during our experiments in the physics lab. It will begin with the thin film Silicon-On-Insulator wafer (TFSOI) on which a layer of silicon dioxide is grown. The sample is then coated with photoresist, which is subsequently exposed through the "base mask" (mask #1) and developed. The SiO_2 is then etched away from the base-diffusion region and remaining photoresist is stripped from the surface. Boron is diffused into the open "window" to form the P-type base and surface is then re-oxidized. Using photolithography once again, the oxide is removed from those regions in which phosphorus is to be diffused using (mask #2) to form the N-type emitter and collector regions. Once phosphorus has been diffused to appropriate depth, the entire surface of the transistor is re-oxidized in preparation for metallization step. The sample is coated with photoresist once more, which is as before exposed through the metallization mask (mask #3) and developed. This time, after the oxide etched away from the designated areas, the photoresist is not removed from the sample's top surface. Aluminum is evaporated onto the entire surface with the resin still on it and the excess Al, which does not cover any contact area, is "floated off". This is done chemically with a solution that "swells up" the resin and dislodges the aluminum from the non-contact areas. This process is known as lift-off. After this process, aluminum is left only in the base, emitter and collector contact regions. The contacts are than alloyed to the Si substrate and device performance is finally tested.

5. CONCLUSION

Summarizing this paper starting with fabrication methods of SOI wafer, we have seen that Silicon– On- Insulator could be produced using SIMOX, BESOI, SEG and ELO. During the work of this paper, we have reviewed the steps of fabrication bipolar transistors on thin film SOI by using planar structure and discussed that the Silicon-On-Insulator (SOI) fabrication process is quickly becoming the answer to the technical challenges facing the integrated circuits (IC) industry.

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