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DESIGN AND ANALYSIS OF FEASIBLE SYNCHRONOUS RECEIVER ARCHITECTURE

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ABSTACT: Wireless communication needs faster speed to give best performance in critical applications. To increase the data rates which is operated under sub millimeter wave range, effective analog synchronous receiver was proposed. This concept neglects the use of feedback loop to the system and follows the feed forward concept. This proposed architecture eliminated many requirements of the conventional technologies like Phase Locked Loop and delay line controller. The proposed deign of Analog Front End have the features of low cost and simple operation. This method also adds the unique feature of phase noise suppression. System level simulations were also presented to check the performance of the feasibility and estimation of performance under several considerations.

Keywords: Phase Locked Loop, Analog Front End, delay line controller, analog synchronous receiver and phase noise suppression

1. INTRODUCTION

Technology is increasing in rapid way from time to time. In wireless communication field, the research is going to achieve data rates of the order of Multi-Gbps. Synchronization and carrier acquisitions are the challenging tasks in achieving the required data rates [12]. If we consider the case of mobile users, it is further difficult to provide Multi Gbps data rates because of their moving nature from time to time. In guided communication, to synchronize and to achieve high data rates the designers used same local oscillator at both transmitting and receiving ends [11]. Due to lack of synchronization, we are not implementing Analog Front End (AFE) model in wireless field [2]. Several researches have been done on the implementation of digital base band receivers which are able to handle target transmission. According to the [1], Application Specific Integrated Circuit (ASIC) and customized Analog to Digital converters were used to design the optical transmitter. By following synchronization in digital domain with the help of Quaternary Phase Shift Keying (QPSK), the designer achieved data rates up to 10Gbps. Implementation of Multi Gbps data rates depends on the performance of Digital Signal Processors (DSP'S) and ADC. It possible to obtain this type of high data rates for the system which is operated based on the millimeter wave length bands [1][9].

2. EXPERIMENTAL RECEIVER ARCHITECTURE

The proposed architecture completely depends on carrier recovery basis. This is a simple and less complex process and follows feed forwarding technique [12]. To acquire perfect synchronization in terms of gain, phase and frequency, conventional receiver architectures followed Phase Locked Loop (PLL) in their design analysis [13,14]. The proposed architecture is exceptional in this one, it didn't use any PLL. Moreover, the conventional receiver structures used Differential demodulators to extract the exact data. The proposed architecture eliminated this concept also [10].

In this method, the process of demodulation is not depending on factors speed of circuitry and frequency of operation [11,12]. This feature will reduce the cost of the process and also implemented with simple technology rather than existed types of CMOS technologies. Noise is the common phenomenon in communication environment. Suppression of noise is always a

challenging task. This proposed method also provided the feature of phase noise suppression [7]. The following figure shows the architecture of analog receiver.

For the above architecture, we used the range of intermediate frequency as 5GHz. This process uses the super heterodyne receiver to reduce the complexity of the system. Receiver receives the signal which has the characteristics of Quaternary Phase Shift Keying with the frequency 60GHz. As shown in the figure, it first enters into the down converter. Down converter has Low Noise Amplifier (LNA) which amplifies the signal. The output of the down converter was given to the IF amplifier. Depending on the range of intermediate frequency, IF amplifier allows the signal which id required [5]. This output of IF amplifier feeds to the two circuits. One output was fed to the demodulator, which is a critical

Figure 1: Analog receiver architecture

element in this process. The other was given to the carrier recovery. Frequency multiplication was used for carrier recovery [6]. The main advantage behind using the frequency multiplication was to generate the harmonics of carrier signal without the process of modulation. Depending on the order of modulation, it may vary as BPSK, 8PSK or 16PSK. From the figure it was observed that, carrier recovery section doesn't have any feedback loop. Whatever, this section will receiver, it has to forward to the next section, and hence it is called as carry forward or feed forward process [4]. To eliminate the modulated content in carry recovery section, we are quadrupled the QPSK signal. Due to the nature of quadrupling, fourth harmonic of the signal was generated. This output signal passed through the band pass filter and also divided by4 [2]. This introduction of division leads to the generation of new IF range. The selection of divider was depends on the designer choice, here we used static frequency dividers. All this process will take certain time and it may cause delay. The designer has to compensate this time delay for proper function of the system [8]. We used phase shifters to compensate the time delay. The output of the phase shifters was given to the demodulator. At the output, we obtain synchronously demodulated base band symbols [9].

The advantages of the proposed architecture were listed below.

- Less hardware utility: Analog Front End was required to match the input signal range to the manageable base band range. To do this process, we just added quadruple and phase shifters. With this less hard ware utility, we achieved the desired range of output [3].

- Digital base band resolution: digital frequency acquisition was eliminated due to the insertion of alternate carrier recovery domain. Digital base band process is used for the defined scenarios only. This complete digital base band was implemented by using 1 bit.

- Phase noise suppression: unique special feature of this process was phase noise suppression. Noise from both frequency synthesizer and receiver was suppressed effectively.

3. SIMULATION ANALYSIS

To verify the performance of the system and to check its compatibility with defined conditions, we simulated by using Agilent Advanced Digital System. This simulation is one of the best tools to implement any behavioral model circuits. We introduced defined channel responses to the system by using MATLAB interface. The following figure 2 shows the simulation setup.
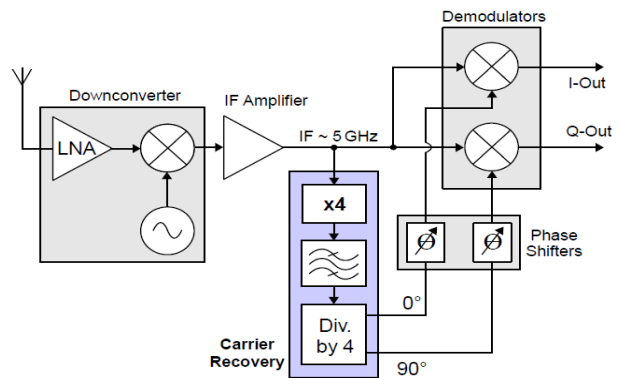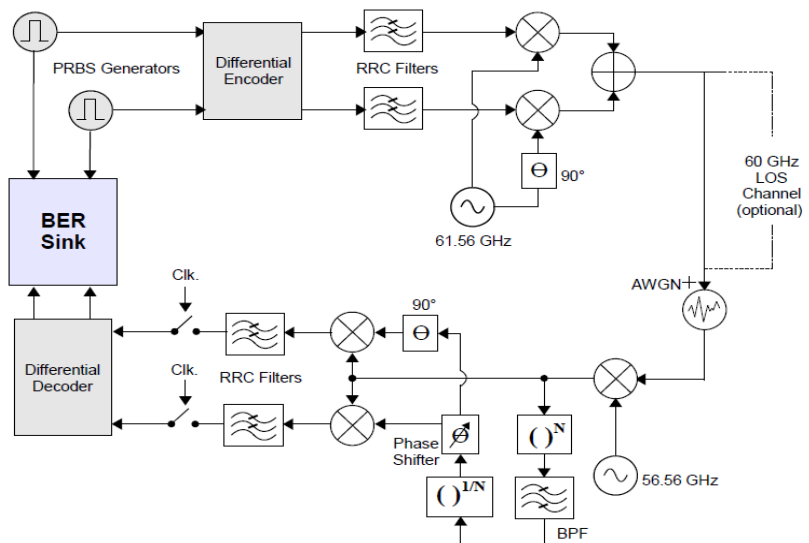

Figure 2: simulation setup for proposed receiver

Two pseudo noise generators were used to generate the transmitted signal with the range of frequency of 60~65GHz. The process of band limitation is mandatory for proper transmission. To do this limitation, we used pulse shaping filters in both transmission and reception. This filter has the roll factor value of 0.34~0.40. The selection of filter is in designer hands, we used Root Raised Cosine (RRC) filters. The modulated signal was generated and it is applied to the receiver using kiosk channel.

The receiver will receives the modulated signal along with the system insertion Additive White Gaussian Noise (AWGN) factor. From the figure 2, it is observable that the selection of PSK was left to user choice. To do simulation, we used N value as 2, which represent the BPSK. Differential encoder and decoder were used to resolve all phase mismatch problems. With the help of Monte Carle simulation tool, BER curves were achieved. For 10^6 symbols, simulation process (QPSK) was performed and results were shown in following figure.

Simulated BER for the values of 3 dB bandwidth for band pass filter was shown in following figure. For comparison, differentially encoded QPSK & BPSK at receiver were shown.

Figure 3: Simulation of input QPSK signal

Figure 4: BER with respect to differentially encoded QPSK & BPSK at receiver

Spectrum of noisy carrier signal was generated under two cases.
1. Bandwidth was constant and noise power will change
2. Noise power was constant and bandwidth will vary.

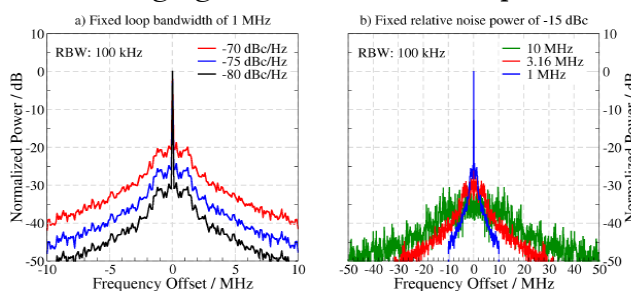The following figure shows simulated spectrum of above two cases.

Figure 5: Simulated spectrum of Noise power and Bandwidth

Figure 6: Simulation results of BER with respect to different delay errors

The following figure shows for the above two cases with respect to BER for different delay errors.
Channel frequency responses were measured under two cases.
Case1: Perfect aligned antenna (1&3)
Case2: Angular mismatch antennas (2 &4)
The following figure shows the channel frequency responses with respect to alignment of antennas.
The following figure shows the performance of BER for 4 defined channel under the same frequency (60GHz).
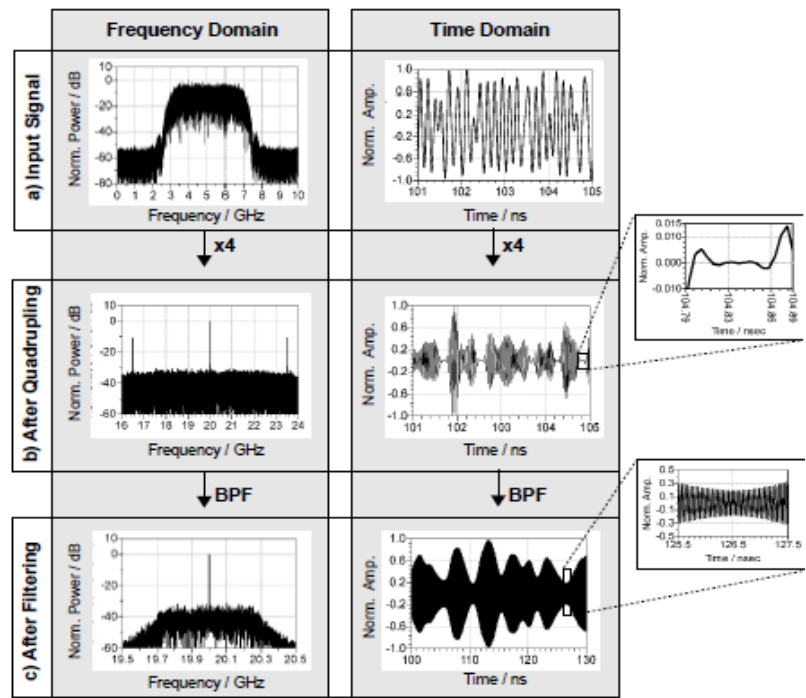
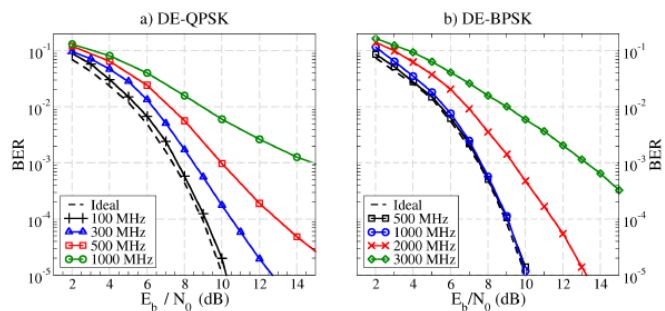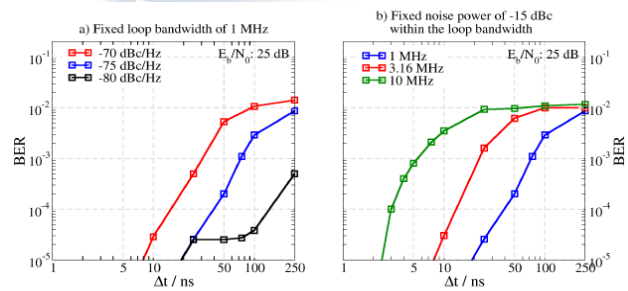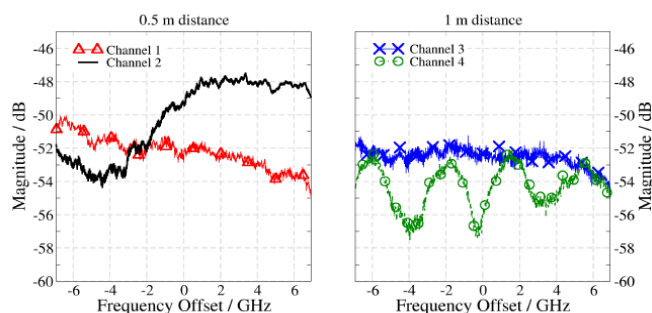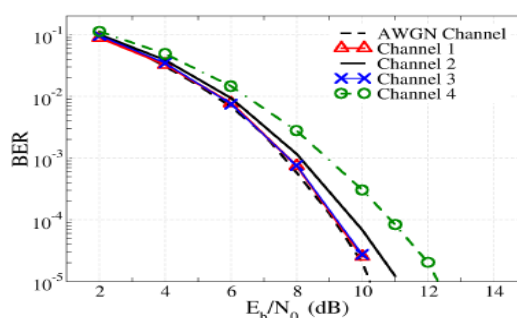**Figure 7**: Frequency responses for different channels   **Figure 8**: BER for 4 different channel responses

CONCLUSION

All simulation results proved that the proposed architecture was effective in terms of many factors. By reducing the system rate, we relaxed the bandwidth requirement up to some extent. Phase noise suppression was ultimate feature which was implemented by using the real time frequency synthesizer. It was also shown that, the proposed receiver architecture was not affected from multi path propagation and also proved to operate with the multi Gbps rate.

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