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ANALYSIS AND REDUCTION OF VOLTAGE RIPPLE IN FORWARD CONVERTER USING A BI-QUAD HF FILTER

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Abstract: Reduction of voltage ripple in forward converter system is discussed in this paper. High power, isolation, transient response, high switching frequency, reduced noises and range of steady state are all necessary requirements for the forward converter. In this paper, a cascaded Bi-quad high frequency filter is proposed and it is used for the forward converter system to reduced the ripple for charging a battery of server SMPS is proposed. In this paper, the proposed converter consists of a NPC-ARS circuit for soft switching on the primary side and an isolation transformer and a rectifier structure on the secondary side. With this modified NPC-ARS circuit topology, soft switching occurs during conversion and reduces the switching loss in this system. A forward converter with RCD snubber, double forward converter and the modified SMPS System are simulated using Matlab-Simulink. FFT analysis for output voltage of LC-filter, π-filter, and cascaded Bi-quad high frequency (CBHF) filter are presented to find the suitable circuit for the SMPS system. The circuit operation, reductions in voltage stress and ripple voltages are described and the simulation results are presented.
Keywords: Ripple voltage, Ripple factor, Bi-quad high frequency (HF) filter, Voltage stress

INTRODUCTION

In recent years, the switching mode power supply (SMPS) system has been achieved with high power density and high performances by using power semiconductor devices such as IGBT, MOS-FET and SiC. However, using the switching power semiconductor in the SMPS system, the problem of the switching loss and EMI/RFI noises has been closed up. This course produced the EMC limitation like the International Special Committee on Radio Interference (CISPR) and the limitation of harmonics for the International standard is Electro technical Commission (IEC). For keeping up with the limitation, the SMPS system must add its system to the noise filter and the metal and magnetic component shield for the EMI/RFI noises and to the PFC converter circuit and the large input filter for the input harmonic current. On the other hand, the power semiconductor device technology development can achieve the high frequency switching operation in the SMPS system. The increases of the switching losses have occurred by this high frequency switching operation. The inductor and transformer size has been reduced by the high frequency switching, while the size of cooling fan could be huge because of the increase of the switching losses.

Our research target is to reduce the ripple and the switching losses in the SMPS system. One method is the soft switching technique and the other method is by proper choosing of filter circuit. This technique can minimize the switching power losses of the power semiconductor devices, and reduce their electrical dynamic and peak stresses, voltage and current surge-related EMI/RFI noises under high frequency switching strategy. This paper proposes a new DC to DC converter topology for PV applications. Its operating principle, static characteristics, comparison analysis between the proposed converter and the Non-Inverting Buck-Boost converter is carried out for three different scenarios are studied. The proposed converter provides higher efficiency than the NIBB converter is presented [1]. An appropriate topology of a ZVS based Phase Shifted full -bridge DC-DC converter is selected based on advantages of reduced switching losses and stresses with fixed switching frequency. A feed forward voltage mode control is utilized which is easier to design and analyze with good noise margin and stable modulation process and improved line regulation are given [2]. This study presents the analysis and design of a novel technique that improves the efficiency of the conventional forward DC-DC converter by reducing switching losses, along with a comprehensive analysis of the circuit and detailed information for designers. A 5 kW step-down prototype is presented [3]. The auxiliary circuit has only passive elements and thus, the control circuit is simple and is like a regular PWM DC-DC converter. The auxiliary circuit provides ZVS condition for primary switch at turn-off instances. A new soft switching forward-fly-back DC-DC converter is proposed [4]. A double-sided LCLC-compensated capacitive structure dramatically reduce the voltage stress in the capacitive power transfer (CPT) system is proposed for the electric vehicle charging applications with improved efficiency are given [5]. The method to step up the voltage gain by reducing the conduction and switching losses are presented [6]. A closed loop model is proposed for the critical applications and the methods to improve the quality by reducing the error are presented [7]. Due to the comparison between the converters, the simulation results of the double forward converter gives better performance is proposed [8]. Comparison between the converters with constant source and with constant load, which is used to check the maximum power transfer to the load is also presented [9]. The new step up and step down method of switching is used to reduce the stress and the comparison between the simulation and experimental results is also presented [10].

The above literature does not deal with the comparison of forward converter using the LC-filter PI-filter and Bi-quad high frequency filter. The above cited papers do not deal with the comparison of FFT analysis, voltage stress and ripple factor and do not identify a converter suitable for SMPS system.

This work aims to develop simulink models for the above forward converter system. A comparison is also done to find the circuit suitable a suitable filter circuit for the SMPS system. The model is designed and developed, which is used to compare it with the simulation results to find the suitable filter circuit for the converter system.

BI-QUAD HIGH FREQUENCY FILTER

This section introduces the proposed cascaded Bi-quad high frequency filter which is illustrated in Figure 1. The filter circuit is composed of two sections, low pass filter and PI-filter for the forward converter system. These two sections are connected in cascaded to reduce the ripple in the output voltage, when compared to the conventional circuit. Bi-quad filter is suitable for the high frequency circuit, hence the node-a and node-c have a known capacitance to ground, and the balanced operation for reducing the ripples and the electro-magnetic interferences (EMI). It is a second order cascaded Bi-quadratic high frequency filter because, it has two reactance elements namely, C1 and C3. The second order transfer function is given as T(s) and the state equations at node-a and node-c. Using the state flow analysis, it synthesizes the circuit by using the transconductance gm. The (1/s) branch is parasitic caps which become ground in very high frequency (VHF), to balance the operation for reducing the ripple, EMI/RF noises in the output. So, the state equation is converted to a balanced gm-c circuit to become a cascaded Bi-quad high frequency filter.

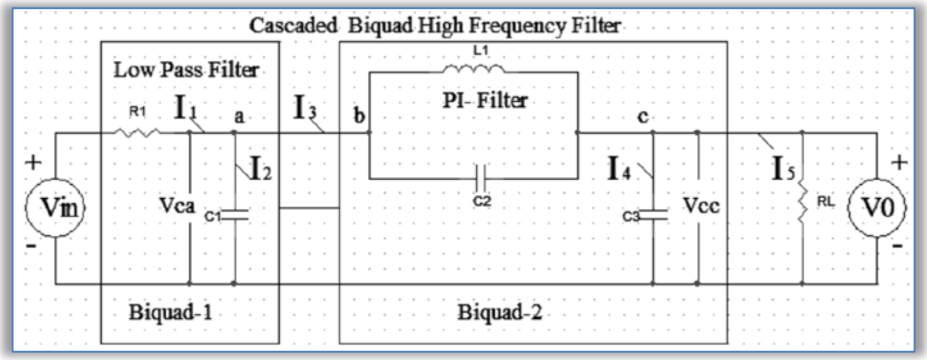

Figure 1. Bi-quad high frequency filter

ANALYSIS

The state flow analyses for the cascaded bi-quad high frequency filter are given below. The Figure 1 is illustrated as cascaded bi-quad high frequency (HF) filter.

The basic general gm-C integrator, control $t_i = C_{eff}/g_{mi}$ by tuning the transconductance. The transfer function suffers from loading effects, which depend on the summation cap C_j. The gain g_m is a design parameter. So, from the basic transconductance (g_m) circuit, the current i = $V_i * g_m$. In general, the m number of capacitance and the n number of transconductance, this is formed as a g_m-c integrator. Then the response of the g_m-c filter is stated as Vo.

$$[VO =]\sum_{i=1}^{n}\frac{gmiVi}{j\omega Ceff}+\sum_{j=1}^{m}\frac{CjVj}{Ceff} \quad (1)$$

where, $C_{eff} = C_{int} + \sum_{j=1}^{m} Cj$

From the state flow at input, V_{ca}:

$$SC_1Vca+I_3L_1+I_3C_2=I_1 \quad (2)$$

$$SC_1V_{ca}+I_3L_1+SC_2\,[V_{ca}-V_{cc}] = [V_{in}-V_{ca}]/R_1$$

$$(SC_1+SC_2)V_{ca}-SC_2V_{cc}+ [V_{ca}/R_1]-[V_{in}/R_1]-I_3L_1$$

$$V_{ca}+ [V_{ca}/S\,(C_1+C_2)\,R_1] = (C_2V_{cc})/\,(C_1+C_2) +V_{in}/SR_1\,(C_4+C_2)-(I_3L_3)/S\,(C_1+C_2) \quad (3)$$

From the state flow at output, V_{cc}:

$$S_{C3}V_{CC}+V_0/R_L=I_3L_1+S_{C2}\,(V_{ca}-V_0) \quad (4)$$

$$S\,(C_3+C_2)\,V_{CC}= [-V_0/R_L] +I_3L_1+S_{C2}V_{Ca}$$

$$V_{CC}= [(-V_0)/S_{RL}\,(C_2+C_3)] + [I_3L_1]/[S\,(C_2+C_3)] + ([C_2V_{ca}]/\,[C_2+C_3]) \quad (5)$$

at node-b, the state I_3L_1:

$$SL_1I_3=V_{ca}-V_0 \quad (6)$$

$$I_3= [(V_{ca}-V_0)]/SL_1 \quad (7)$$

This circuit is composed of low pass filter and PI-filter with the parasitic caps are connected in cascaded to formed as a bi-quad high frequency filter, which is to reduce the ripple in the output voltage.

SIMULATION RESULTS

The SMPS system is modeled and simulated using the blocks of MATLAB SIMULINK. The SMPS system using forward converters with RCD snubber, double forward converter and the modified forward converter using LC-filter, π-filter and high frequency cascaded filter are simulated, and the results are presented. The voltages measured at node-a, represents the voltage across the LC-filter, node-b represents the voltage across the π-filter and node-c represents the voltage across the high frequency cascaded filter.

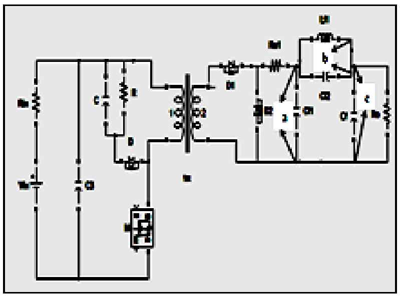

Figure 2a.Forward converter with RCD snubber using cascaded Bi-quad HF filter

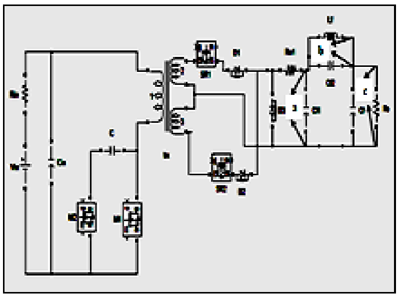

Figure 2 b. Double forward converter using cascaded Bi-quad HF filter

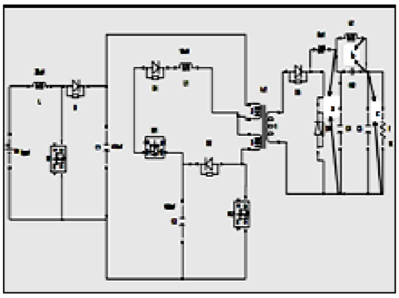

Figure 2c.Modified forward converter using cascaded Bi-quad HF filter

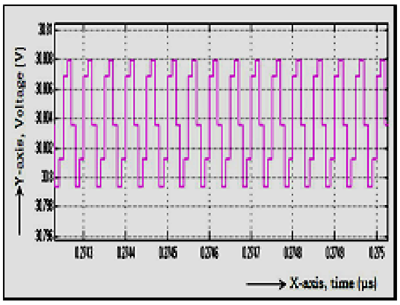

Figure 2 d. The output voltage at node-a for the forward converter with RCD snubber

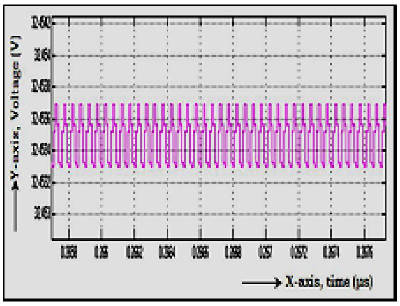

Figure 2 e. The output voltage at node-b for the forward converter with RCD snubber

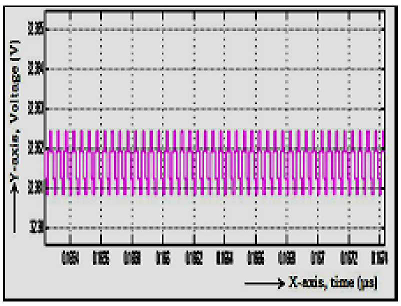

Figure 2 f. The output voltage at node-c for the forward converter with RCD snubber

The forward converters with RCD snubber using high frequency cascaded filter is shown in Figure 2a. The double forward converters using high frequency cascaded filter is shown in Figure 2b. The modified forward converters using high frequency cascaded filter is shown in Figure 2c. Figures 2d-2f represents the output voltage at node-a to node-c for the forward converters with RCD snubber. Figures 2g-2i represents the output voltage at node-a to node-c for the double forward converters. Figures 2j-2l represents the output voltage at node-a to node-c for the modified forward converter.

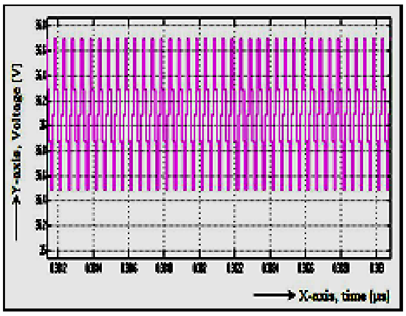

Figure 2 j. The output voltage at node-a for the modified forward converter

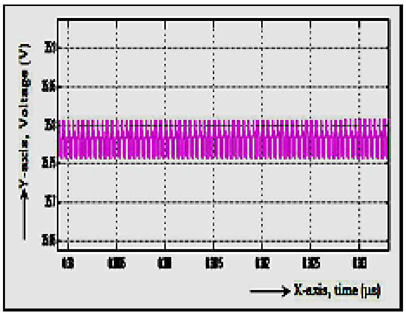

Figure 2 k. The output voltage at node-b for the modified forward converter

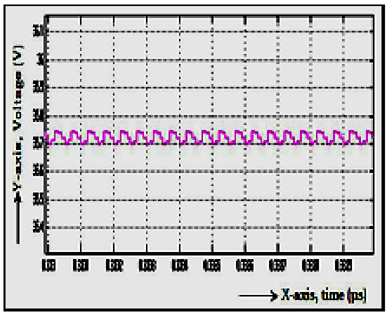

Figure 2 l. The output voltage at node-c for the modified forward converter

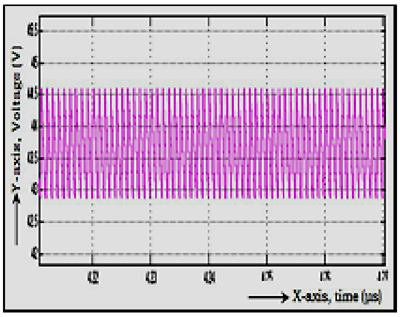

Figure 2 g. The output voltage at node-a for the double forward converter.

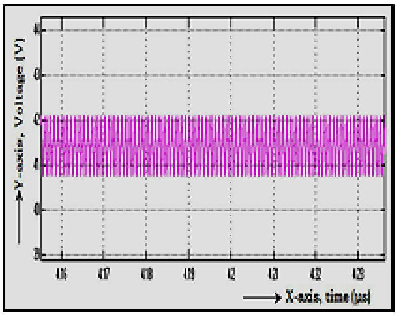

Figure 2 h. The output voltage at node-b for the double forward converter.

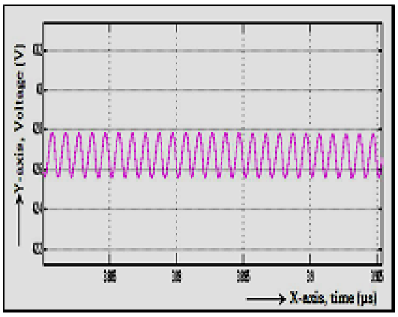

Figure 2 i. The output voltage at node-c for the double forward converter

FFT analysis for output voltage of forward converter with RCD snubber, double forward converter and the modified forward converter is shown in Table 1. Summary of voltage ripple and percentage of ripple factor by using the LC, PI and HF cascaded filter are shown in Table 2.

Table 1. Summary of FFT analysis of output voltage for the three converters system.

S.No:	Frequency (KHZ)	RCD Snubber Output Voltage (V)			Double forward converter Output Voltage (V)			Modified forward converter Output Voltage (V)		
		LC Filter	Π Filter	Cascaded Filter	LC Filter	Π Filter	Cascaded Filter	LC Filter	Π Filter	Cascaded Filter
1.	0 KHZ	33.5	33.2	33.3	26.64	33.4	38.1	46.5	75.7	40.5
2.	40 KHZ	5.77	5.02	2.62	6.64	3.81	2.54	5.37	2.15	1.53
3.	80 KHZ	2.11	2.18	0.64	3.09	1.50	0.83	2.67	0.50	0.35

Table 2. Summary of ripple voltage and percentage of ripple factor with different filters.

S.No:	Parameter	LC Filter	Π Filter	HF Filter	LC Filter	Π Filter	HF Filter	LC Filter	Π Filter	HF Filter
1.	Ripple Voltage	6.07	5.4	2.6	7.2	4.0	2.6	5.90	2.15	1.52
2.	% of Ripple factor	18.1	15.1	6.0	26.9	12.1	6.9	10.8	2.9	2.5

Table 3. Summary of voltage stress for the three converters system

S.No:	Parameter	RCD Snubber		Double forward converter		Modified forward converter	
		Without ZVS dv/dt	With ZVS dv/dt	Without ZVS dv/dt	With ZVS dv/dt	Without ZVS dv/dt	With ZVS dv/dt
1.	Voltage Stress	$0.4*10^6$ V/Sec	$0.2*10^5$ V/Sec	$0.8*10^6$ V/Sec	$0.6*10^5$ V/Sec	$0.5*10^6$ V/Sec	$0.3*10^4$ V/Sec

The voltage stress with and without dv/dt for the forward converter with RCD snubber, double forward converter and the modified forward converter is shown are Table 3. Comparison of regulation and output power for the forward converter with RCD snubber, double forward converter and the modified forward converter are shown in Table 4. From the comparison of regulation, it is observed that the double forward converter has good regulation and from the comparison of output power, it is clear that the modified SMPS system using neutral point connected to the auxiliary resonant snubber circuit delivers higher power in the SMPS system.

Measurement of efficiency for the constant source with constant load is shown in Table 5. From the comparison of efficiency, it is clear that the modified SMPS system using neutral point connected to the auxiliary resonant snubber circuit delivers higher power in the SMPS system.

Table 4. Comparison of regulation and output power for the forward converters system

S.No:	Converter Models	Comparison of Regulation			Comparison of output power		
		Voltage drop	Voltage regulation	% of voltage regulation	Output voltage	Output current	Output power
1	Forward converter system	0.9	0.022	2.25	39.31	0.78	30.9
2	Modified SMPS system	7.9	0.19	19	42.68	0.865	36.67
3	Double forward converter system	0.5	0.012	1.25	40.57	0.81	32.92

Table 5. Comparison of efficiency

S.No:	System with constant source and constant load	Input voltage	Output voltage	Efficiency
1.	Forward converter with RCD snubber	100	39.31	39.31
2.	Modified SMPS system	100	42.68	42.68
3.	Double forward converter	100	40.57	40.57

Table 6. Comparison of efficiency for variable input voltage

S.No:	System with variable source	Input voltage	Output voltage	Efficiency
1.	Forward converter with RCD snubber	50	19.01	38.02
		100	39.31	39.31
		150	58.58	39.05
		200	78.36	39.18
2.	Modified SMPS system	50	19.54	39.08
		100	42.68	42.68
		150	68.69	45.79
		200	96.57	48.28
3.	Double forward converter	50	19.79	39.58
		100	40.57	40.57
		150	60.34	40.22
		200	80.62	40.31

Forward converter system with variable source and its efficiency for the three converters are shown in Table 6. From the comparison it is clear that the modified SMPS system using neutral point connected to the auxiliary resonant snubber circuit delivers higher power with efficiency in the SMPS system.

CONCLUSION

The forward converter with RCD snubber, modified system with NPC-ARS circuit and the double forward converter circuit were modeled with LC-filter, Π-filter and the cascaded filter which were simulated using simulink. FFT analysis of output voltage of the filter, ripple voltage, percentage of ripple factor and the reduced voltage stress were obtained. Summarizing what is aimed at and what is achieved, in the present work, it was not just the simulation of forward converter circuits but also the by investigating the different forward converter configurations, it was seen that the double forward converter circuit was most suitable for the SMPS system, since it had good voltage regulation and reduced steady state error.

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