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VERIFYING THE FUNCTIONALITY OF A PARALLEL-SERIES CONVERTOR USING NEXIS 4 DEVELOPMENT BOARD

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Abstract: The paper presents a parallel series 8-bit converter. The scheme is carried out and implemented in the Xilinx on-board Nexis4DDR. The scheme comprises two 4 bit counters, and a parallel input shift register and a schematic performed in the frequency divider done in VHDL. The sequence of the required clock is obtained by dividing the clock frequency of 100 MHz on-board by means of a division circuit which allows setting the required frequency soft.
Keywords: Shift registers, Complex logic circuits, Field programmable gate arrays, Nexis 4 DDR

1. INTRODUCTION

The parallel series converter was implemented in Xilinx ISE. This is a design environment integrated digital systems implemented on programmable circuits XILINX, which offers a wide range of applications using FPGA or CPLD design. The design can be achieved using both describing schematic and hardware description languages (VHDL or Verilog) [1] [2] [3].

After the implementation of logic circuits and verify their correctness and setting files constraints, program Digilent Adept System file extension .bit registers on Nexis4DDR. (Figure 1)[4]

The Nexys 4 DDR board is a complete, ready-to-use digital circuit development platform based on the latest Artix-7 Field Programmable Gate Array (FPGA) from Xilinx. With its large, high-capacity FPGA, generous external memories, and collection of USB, Ethernet, and other ports, the Nexys4 DDR can host designs ranging from introductory combinational circuits to powerful embedded processors.

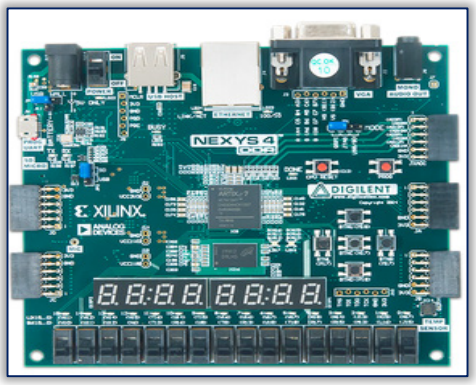

Figure 1. Nexis 4DDR board

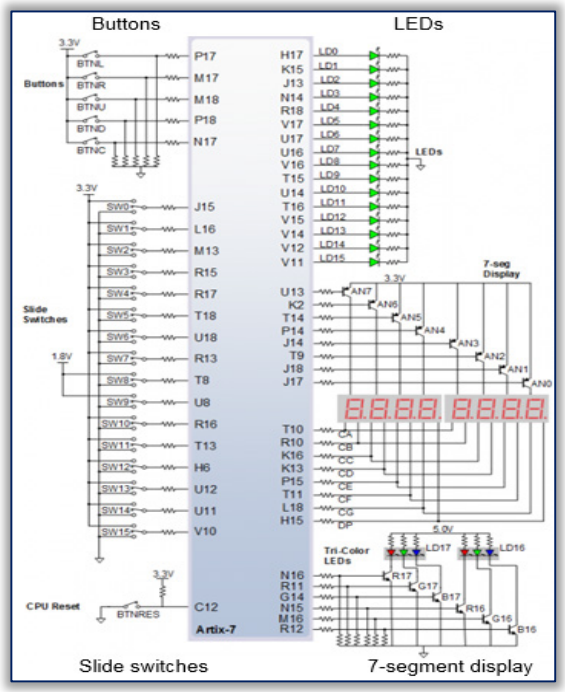

Figure 2. I/O circuits of Nexis 4DDR board

Usually, the Nexis 4 DDR board is powered via a USB cable, but it is also fitted with a connector for an external power source, for example a battery of 3.5 V – 5.5 V.

The Nexis 4DDR board contains: 15,850 logic slices, each with four 6-input LUTs and 8 flip-flops 4, 860 Kbits of fast block RAM, internal clock speeds exceeding 450 MHz, on-chip analog-to-digital converter (XADC), USB-UART Bridge, 12-bit VGA output, Digilent USB-JTAG port for FPGA programming and communication, four Pmod ports and other.

The Nexys4 DDR board includes two tri-color LEDs, sixteen slide switches, six push buttons, sixteen individual LEDs, and an eight-digit seven-segment display, as shown in Figure 2. [4]

The pushbuttons and slide switches are connected to the FPGA via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output). The five pushbuttons arranged in a plus-sign configuration are "momentary" switches that normally generate a low output when they are at rest, and a high output only when they are pressed.

The red pushbutton labeled "CPU RESET," on the other hand, generates a high output when at rest and a low output when pressed. The CPU RESET button is intended to be used in EDK designs to reset the processor, but you can also use it as a general purpose pushbutton. Slide switches generate constant high or low inputs depending on their position.[4]

2. DESCRIPTION OF APPLICATION

The operating principle of the proposed system is based on the block diagram (Figure 3), containing the main modules created in Xilinx. [5]

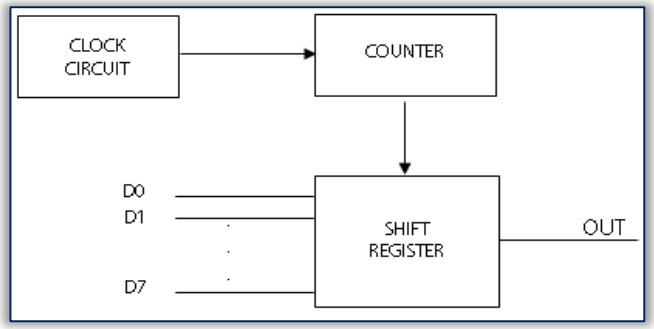

Figure 3. The block diagram of the system

The tact circuit necessary to control parallel-serial conversion is implemented in VHDL code. (Figure 4) The program performs a division of the clock frequency of 100 MHz on Nexis plate 4 at the desired frequency for controlling the DDR data conversion.

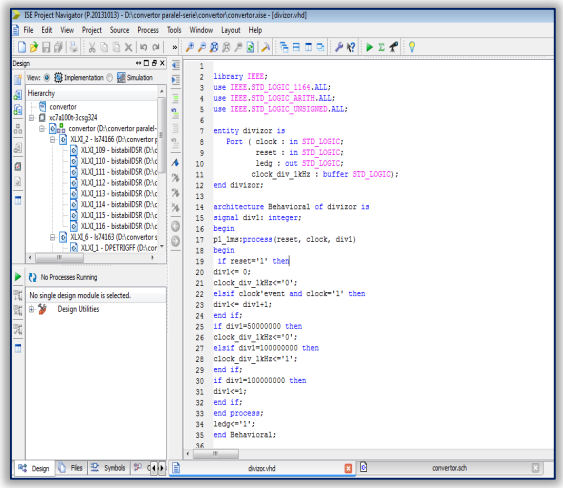

Figure 4. Clock circuit created in Xilinx

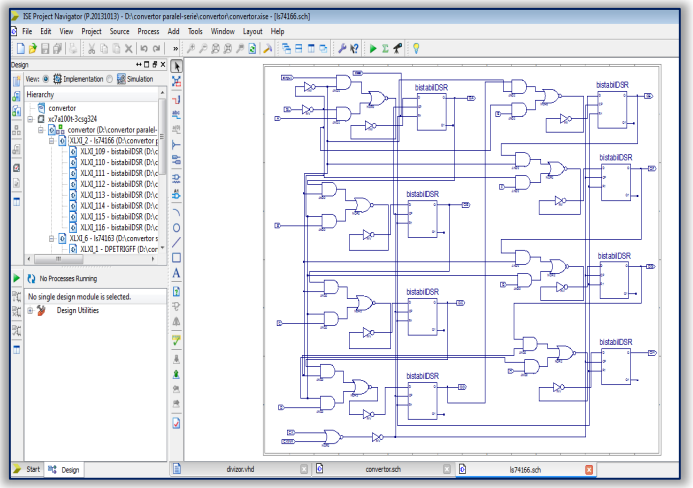

Figure 5. Shift register created in Xilinx

We have also built the shift register structure (Figure 5) and the related constraints file (Figure 5), followed by the verification of operation using the Nexis4DDR board.[5][6][7][8]

Based on the results, we obtained the shift register schematic symbol, used subsequently in the final circuit.

The counting block contains two 4 bit counters connected in series and a SI-NU three-input circuit which commands the end of a byte conversion. Counters (Figure 6) are carried out with JK flip-flop circuit that connected into the structure of the Delay-MS.[8][9]

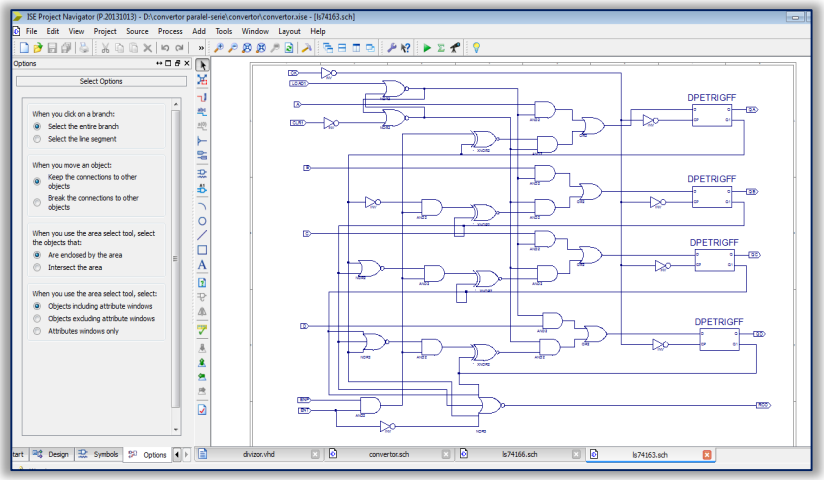

Figure 6. Counter created in Xilinx

The sequence of the input data in the shift register is loaded on its parallel input. The transfer of serial data at output is done one bit at each clock pulse. The end conversion of a byte is controlled by the SI-NU circuit with three inputs which controls the reset of the shift register 111 when the output frequence identifying the first 4-bit binary numbers. Other outputs of the counters provide information about the number of time division serial converted data sequence. The end of such a process is indicated by the SYNC output timing of the second numerator. The frequency control data conversion is obtained by dividing the clock frequency of the circuit board 4DDR Nexis to a desired value according to the actual application in which the parallel-serial conversion circuit is used.

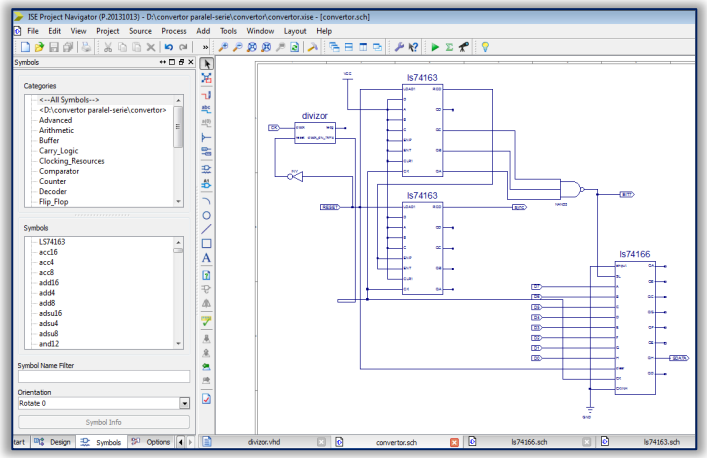

Figure 7. Parallel series conversion circuit made in Xilinx

The operation of each block was independently verified by viewing the Nexis 4 board's output blocks assigned LEDs.After checking the functionality of the blocks circuit symbols were created corresponding to each block separately and the final scheme of the converter was created. The checking of the conversion circuit on Nexis 4DDR board is done by using a lower frequency assignment accessible to the human eye at the output of a LED circuit in the frequency of 1 KHz respectively for viewing the serial sequence at an oscilloscope. Checking the operation of each block in part is presented hereafter. Thus it can be seen the operation of the frequency divider (Figure 8) which must obtain the desired clock frequency for the conversion of the input data. The verification is done at a frequency of 1 Hz to be visually followed and a LED lighting a notice was assigned at the output of the divider. [8][9]

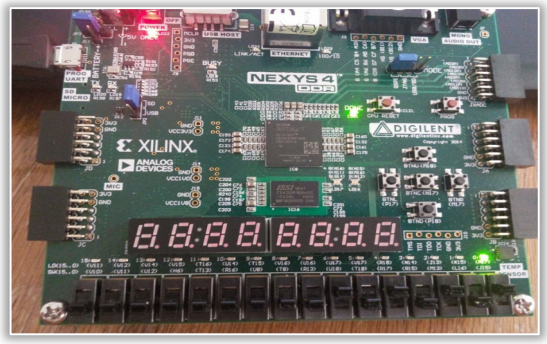

Figure 8. Checking the functionality of the frequency divider

Checking the operation of the counters (Figure 9) outlines the lighting of two LEDs that are properly assigned at the synchronization signals and at end of the conversion of a byte shift which commands the register's reset. Checking the operation of the shift register (Figure 10) is made by viewing and other circuit blocks, respectively by the turning on of the three LEDs corresponding to each block separately. The verification was done in all presented cases, with entrance represented a byte of eight 1 logic.

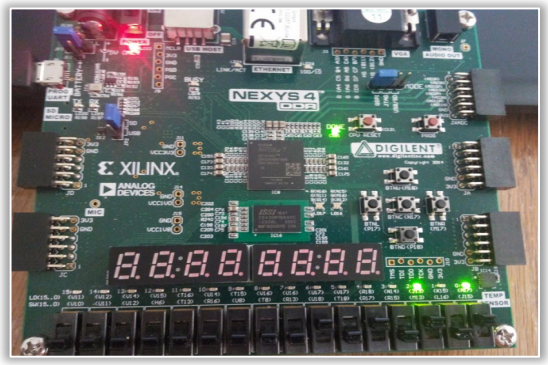

Figure 9. Checking the functionality of the counters

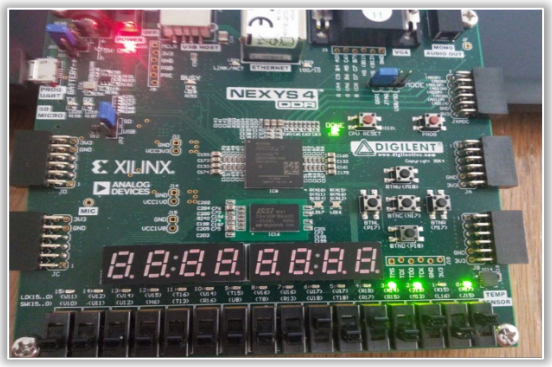

Figure 10. Checking the functionality of the entire module

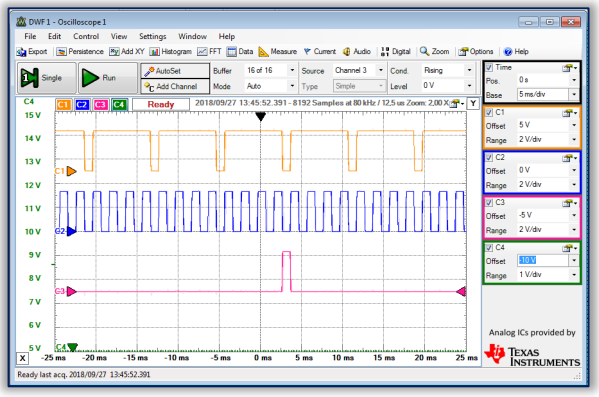

Figure 11. The representation synchronization signals, output and end of frequency conversion at 1 kHz

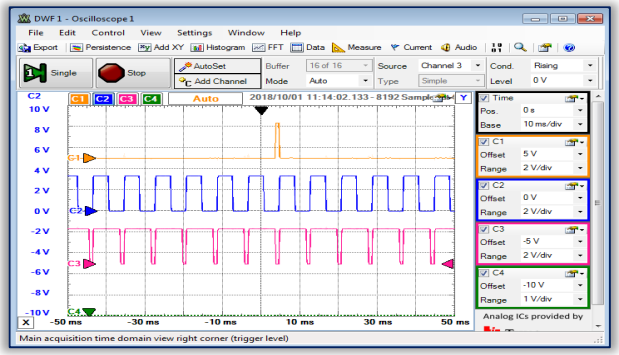

Figure 12. Representation of synchronization signals, output and end at 1 kHz frequency conversion, sequence data for 1111000

Checking the operation of the conversion circuit (Figure 11) at a frequency of 1 kHz with a data sequence composed of 4 byte of 0 and 1 alternative 4 (10101010).
The synchronization signal is activated at the end of the counting sequence of the counter 2 after 32 bytes. The sequence data is presented in the succession of 1's and 0's during the counting sequence of the counter circuit 1 that by identifying the condition 111 to the three outputs A, B, C commands the reset of the shift register.
The other structure of the input data (Figure 12) consists of four 1's and 0's 4 (11110000) at the same frequency of 1 kHz, it is found normal operation of the conversion circuit.

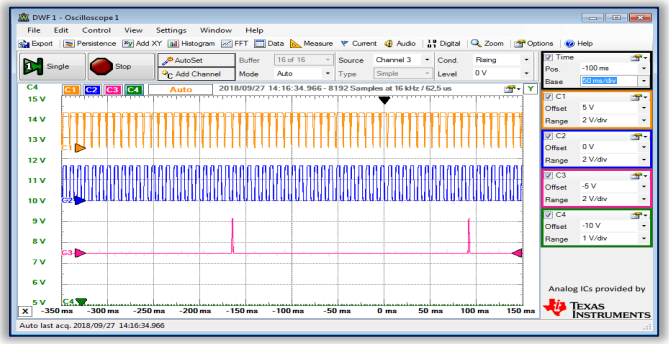

Figure 13. Viewing sequences output during a full system of counting

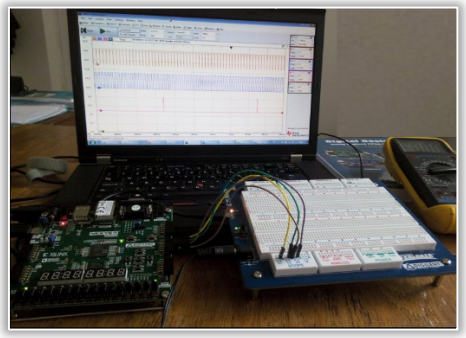

Figure 14. Viewing the output signals by using the Electronics Explorer Board module

For sequence data previously presented (11110000) at 1 kHz frequency are presented (Figure 13) sequences at the output sequence between two synchronization signals which are activated every 32 bytes determined by the ending signal of a byte conversion.
How to collect output signals are presented in figure 14 which shows the connection board Nexis 4DDR to the Electronics Explorer Board module.

3. CONCLUSIONS

An advantage of the Xilinx program is its flexibility, but also the fact that we can relatively easily develop projects just using the library of the program. Other advantages are its high programmability and low time required for design and presentation of the product on the market.
Also, the program has an IEEE standard recognized by all manufacturers.
The FPGA devices enable the design of specialized hardware architectures, thanks to the flexibility advantage of the programmable environment in which the implementation is carried out. This provides an extra degree of freedom in the design of digital control systems compared to the use of microprocessors, because the hardware architecture of the control system must not be imposed previously.
The circuit conversion enables the transfer of a byte in serial format, transfer which can be carried out with a rate of software command transfer by suitably changing the output frequency of the frequency divider, the frequency of which is obtained by dividing the corresponding frequency of 100 MHz on board Nexis 4 DDR. This frequency commands the data transfer rate when exiting the parallel-serial shift register. The identification circuit at the output of counter 1 sets the end of conversion for each octet. In this paper is presented the function conversion circuit at two frequencies, but it can be checked any frequency less than 100 MHz that is a whole submultiple of this value and which can be achieved by programming the Xilinx software. Serial output signal from the logic circuit can control any compatible Nexis 4 DDR board.

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