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USING THE MATLAB-SIMULINK SIMULATION FOR OPERATING ACTIVE FILTERS ORDERED BY DIGITAL SIGNAL PROCESSOR (DSP)

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ABSTRACT: The paper proposes the use of a DSP family ADMC330 several ways to control an active filter. It is made available as filter simulation in Matlab-Simulink environment, and the results confirm the effectiveness of the filter. This paper presents four schemes using both types of construction, with and without feedback loop, for three-phase voltage sources but balanced nonlinear load (no neutral wire).
KEYWORDS: DSP family, simulation, Matlab-Simulink

❖ INTRODUCTION

Figure 1 is a schematic diagram of a DSP controlled active filter. The Rp resistors are denoted preloading the filter capacitor C, necessary to limit the current drawn from the converter to the mains connection.

Signals from voltage / current transducers are taken through LEM type, and block 'Adaptation Signals' are made in the range of 0.3 - 3.2 V analog converters acceptable entry - digital. To order using a digital converter evaluation board CMDA signal processor 330 - control processor specifically designed for electric cars.

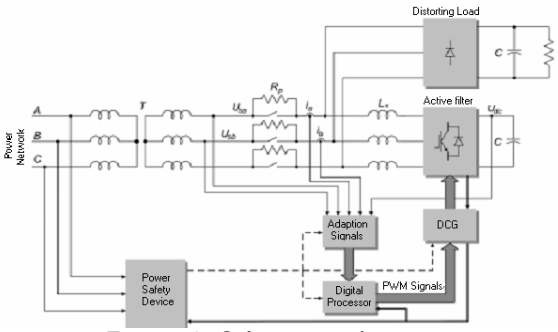

Figure 1. Schematic diagram

ADMC330 microprocessor family is part of the signal processor (DSP) which operates fixed-point math calculations. It's characteristics is recommended for high performance control of electrical drives. Among these we mention below the most important:

- ☐ 20 MHz clock frequency;
- ☐ Seven analog inputs for external signal acquisition;
- ☐ Data acquisition synchronized with the PWM signal;
- ☐ Control signal generator for PWM voltage inverter (Pulse width modulation in - pulse width modulation)
- ☐ Programmer detection dead time and minimum pulse;
- ☐ Minimum inverter frequency 2.5 kHz;
- ☐ Maximum inverter frequency 25 kHz;
- ☐ Generator for the space vector control inverter;
- ☐ Program counter and address two generators;
- ☐ Two 8-bit timers for PWM generation;
- ☐ Eight ports of entry and exit;
- ☐ Implementation of 20 MIPS (million instructions per second);
- ☐ Arithmetic logic unit for executing mathematical calculations;
- ☐ Mathematical operands displacement unit;
- ☐ 50 ns instruction cycle time;
- ☐ Type 16-bit timer watchdog to reset the DSP;
- ☐ Two synchronous serial ports;
- ☐ 2k x 24 bit program memory and data RAM 1k x 16 bits;
- ☐ 2k x 24 bit program memory ROM.

The flexibility of the internal structure ADMC330 signal processor, allow for the following operations in a machine cycle (50 ns)

- ☐ Generating new program addresses;
- ☐ Taking the next instruction stack;

- Achieving two data moves;
- Loading two data pointers with addresses;
- Performing a calculation operation.

The processor can also independently control the peripherals that are fitted, so while it may do the following:

- Generation of three PWM signals for inverter;
- Generation of the two auxiliary PWM signals generators;
- The acquisition of four analog channels;
- Control of eight digital input / output pin;
- Decrementing timer control program (Watchdog).

ADMC330 processor includes internal memory as we have seen, so the 2K monitor ROM program is to interface with a PC UART for serial communication interface, boot loader, mathematical tables to implement the following functions: sine, cosine, tangent and inverse tangent, logarithm and inverse logarithm, square root, inverse function, divide unsigned, transformations from Cartesian to polar marker, functions for interpolation.

❖ SOFTWARE SIMULATION SYSTEM USING MATLAB-SIMULINK

Four schemes were carried out using both types of construction, with and without feedback loop, for three-phase voltage sources but nonlinear loads balanced (neutral wireless). The first two schemes will be presented using real-time Fourier analysis of the currents on each phase.

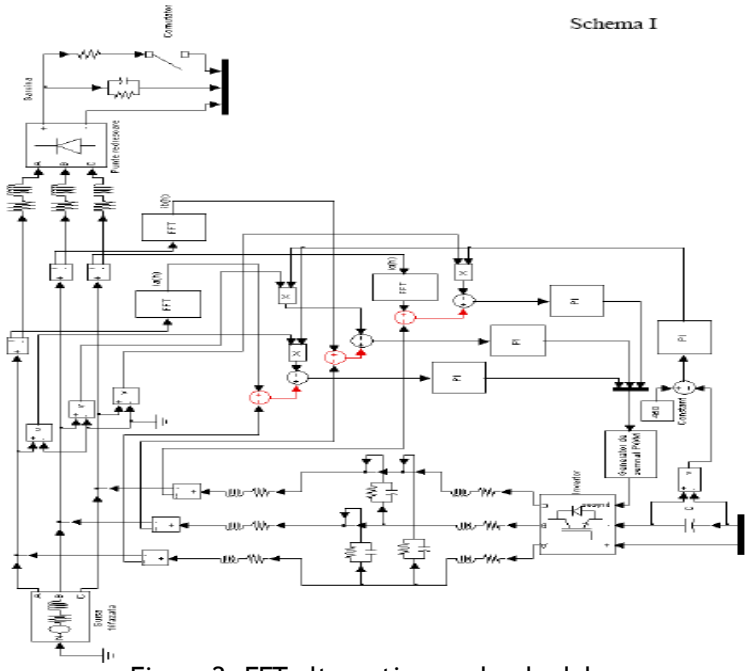

Figure 2. FFT alternative work schedule

Fourier transform is calculated using the fastest FFT algorithm. By Fourier analysis of the currents on each phase has succeeded in its breakdown of its component harmonics. Recomposed signal using only the higher order harmonics (less than first harmonic), it is a signal that will be introduced in the network with the sign reversed. So the grid will run a first harmonic signal. This method is applied to the first scheme.

A second solution is to calculate only the fundamental harmonic is then subtracted from the total current network to produce the higher harmonic current is given by the opposite sign is the reference active filters. Such an approach is adopted in the sliding mode option, which is shown in diagram two.

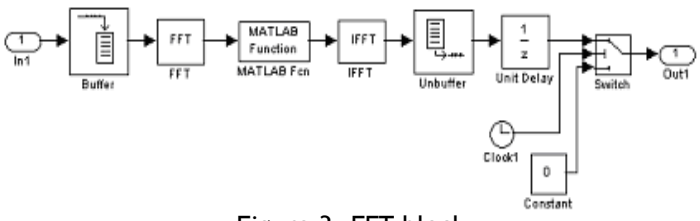

Figure 3. FFT block

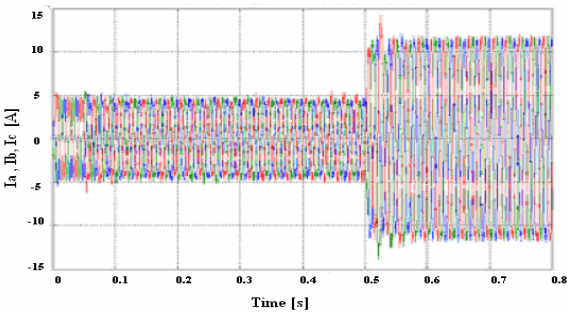

Figure 4. The mains currents

In the following we present diagrams made for each model calculation and simulation results obtained. FFT block in the current decomposition of its component harmonics. Computer program called the block "MATLAB Function" allows the extraction of harmonics first. IFFT block recomposed signal using only higher order harmonics, resulting in a signal that will be introduced in the network with the sign reversed.

Below are the results obtained by simulation.

In Figure 4 the currents are presented mains throughout the simulation period. In the interval (0 - 0.1) current network is not filtered, at time 0.1 comes into the active filter. 0.5 At the burden is doubled.

In Figure 5 phase currents are given power to the system without active filter. It can be seen as their harmonic due to the presence of higher order harmonics.

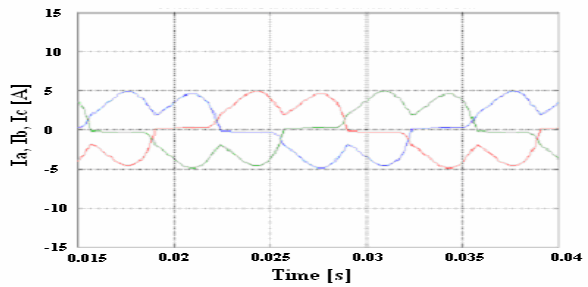

Figure 5. The mains currents without filter

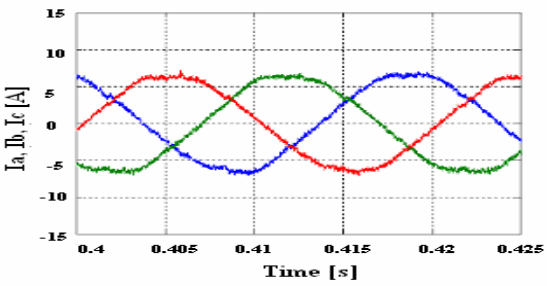

Figure 6. The mains currents active filter

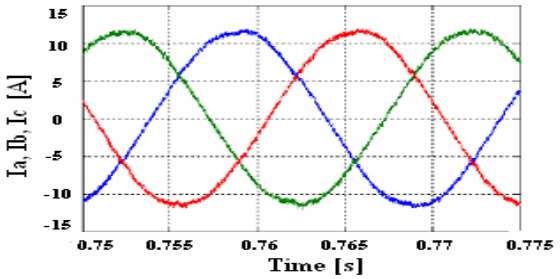

Figure 7. Power supply currents

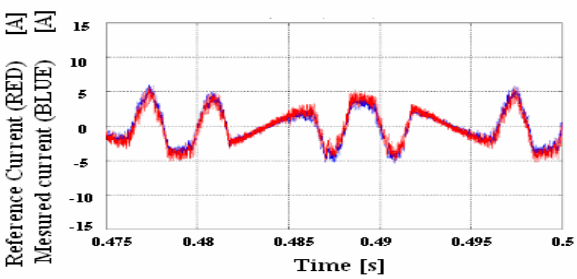

Figure 8. Current compensation the double burden

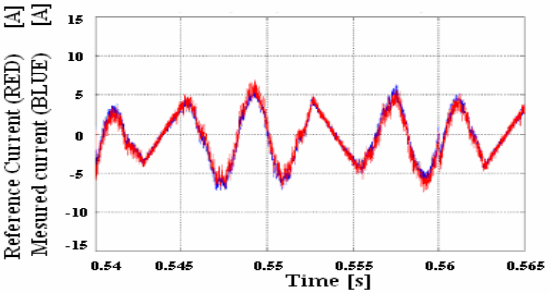

Figure 9. Current produced by the active filter compensation

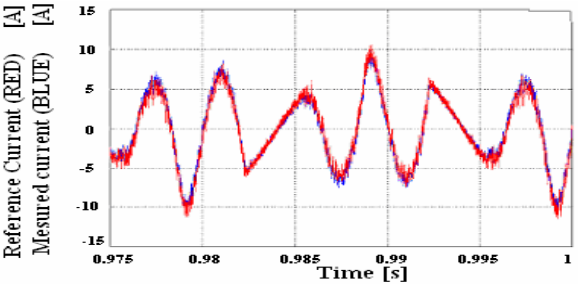

Figure 10.Curent double load compensation

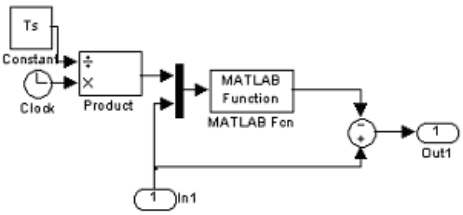

Figure 11. Sliding FFT block

Extract the first harmonic sliding FFT block which then decreased the current network consists of harmonics resulting in a higher power.

In the following we present scheme for model calculation carried in variant sliding mode.

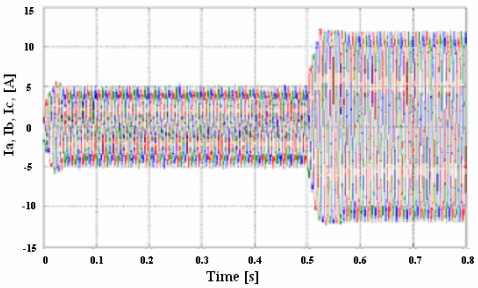

Figure 13. The mains currents throughout the simulation time

In Figure 13 currents are presented mains throughout the simulation period. Results obtained from simulation with the sliding mode

From Figure 6 can be observed that with the arrival of an active filter, three-phase currents are sinusoidal mains.

In Figure 7 we presents three mains currents, the active filter for a dual task.

In Figures 8 , 9 and 10, the reference current (red) are harmonics with opposite sign that must be placed on the network. The blue is injected currents in inverter network.

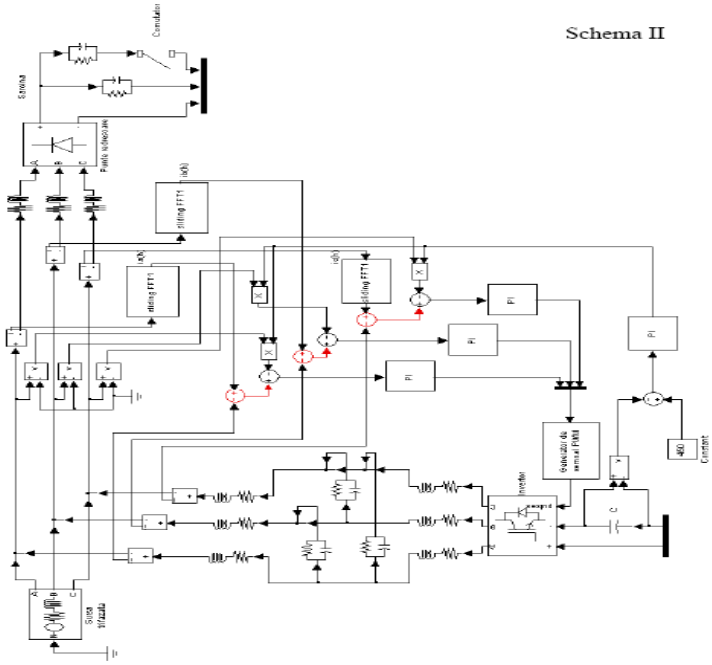

Figure 12. Alternative work schedule with sliding FFT mode

method are similar to those obtained in the FFT version. The only notable difference is that there is an increasing burden smooth current growth.

Unfortunately, this method has the disadvantage that it requires real-time applications using DSP with large memory. This leads to the impossibility of using cheap DSP having more than one Kb of RAM. In this case we propose another solution that enables the calculation based on the fundamental harmonic active and reactive power (by averaging the instantaneous value).

In the following experimental results will be presented.

On the basis of this technique is that transfers of active and reactive power defined as the product of the fundamental harmonic voltage and currents is real only on the first harmonic current harmonic currents rest do not give power. Unfortunately, in some applications the source voltage contains higher harmonics. For this reason the calculation of power is no longer used that tension, but tension given by a PLL circuit realized by software and implemented on a DSP which provides as output a sinusoidal signal in phase with the fundamental harmonic amplitude equal to unity. This signal is subtracted from the total current network to produce the higher harmonics given the current reference is changed in sign of active filter.

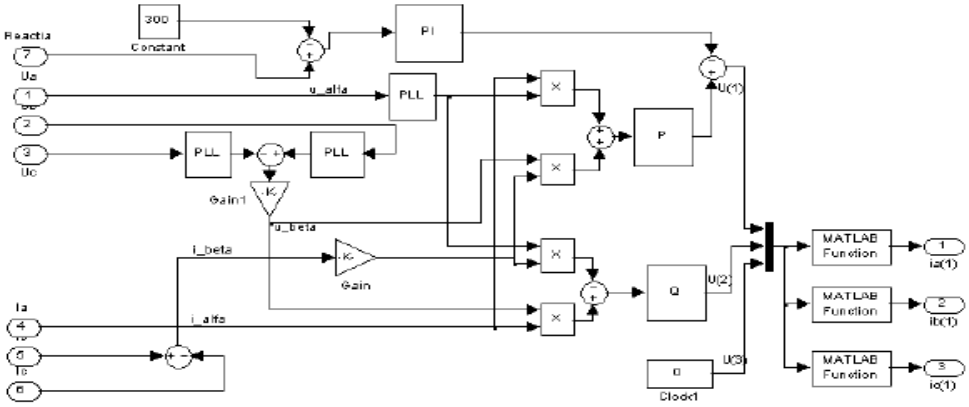

Figure 14. PQ Building

In this block currents and voltages are introduced in three phases. Calculate the first-order harmonic currents. They will then be subtracted from a signal resulting network consists of higher order harmonics to be introduced into the network with the sign reversed.

In Figure 15 PLL block is presented which provides as output a sinusoidal signal in phase with the fundamental harmonic amplitude equal to unity.

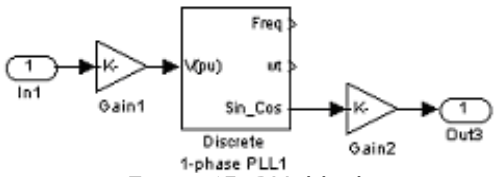

Figure 15. PLL block

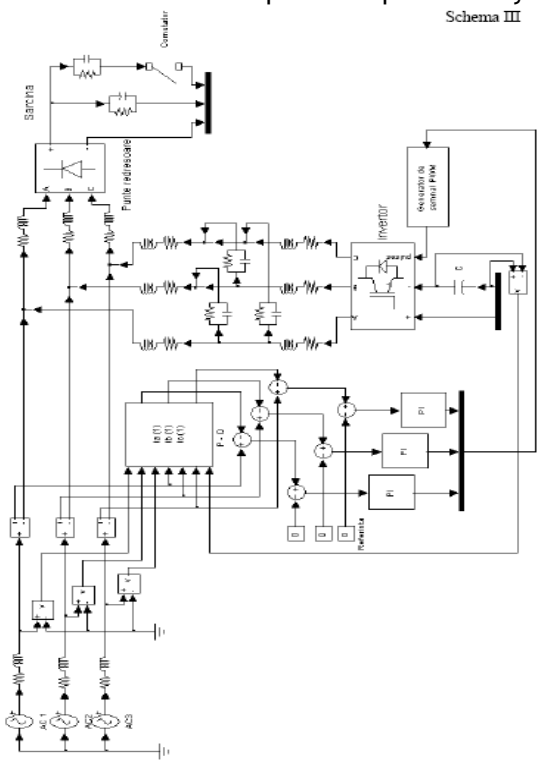

Figure 16. Alternative work schedule PQ-loop response

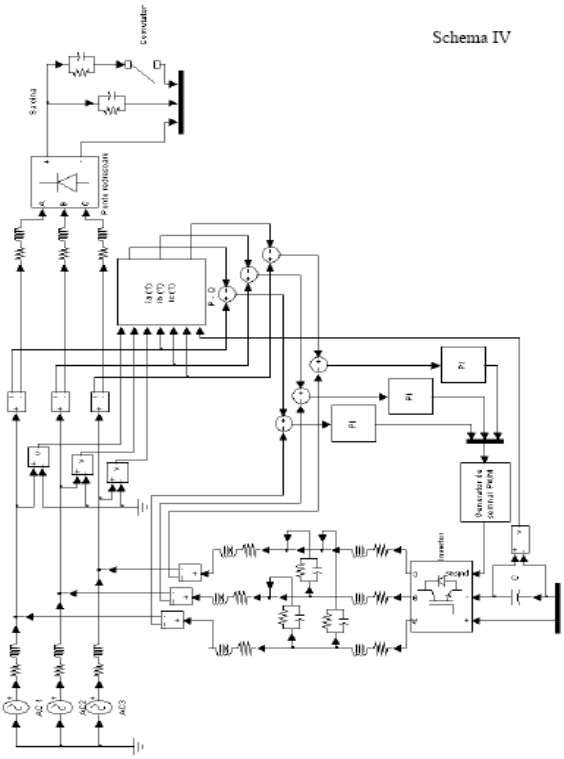

Figure 17. PQ alternative work schedule without feedback loop

Have been developed for this model two types of construction, with and without feedback loop. In the following we present schemes for the two models made constructive and results obtained from simulation. The former alternative presented feedback loop variant.

Results will be presented in the following experimental. In Figure 16 currents are presented mains throughout the simulation period. Note that at time 0.3 with a double load variation occurs due to sudden changes in voltage on the load current, the variation is shown in the figure below. This surge current limiter can be removed from power.

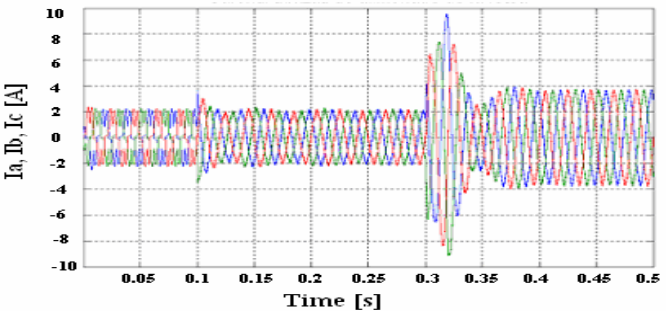

Figure 18. Mains currents throughout the simulation time

Block P-Q is presented in Figure 17. The difference between the two modes of constructive notice is observed in the manner of placing the measure voltages and currents in relation to the inverter, and how the taxation of reference. Figures 18, 19 and 20 are shown the three phase currents at different moments in time simulation.

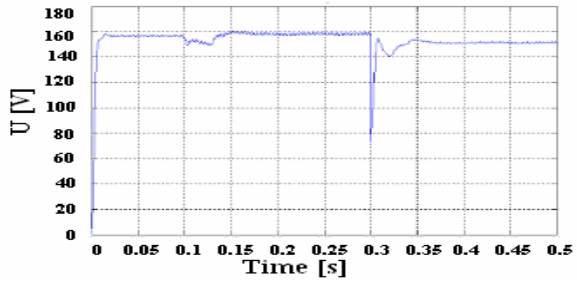

Figure 19. Voltage on the load the mains supply without active filter

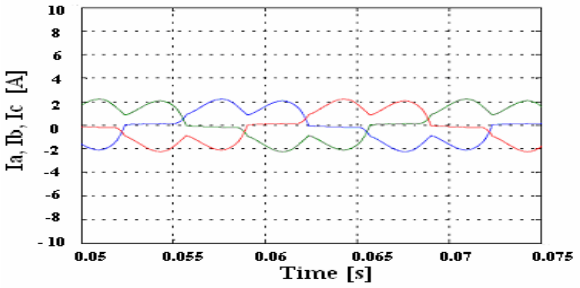

Figure 20. Three-phase currents from

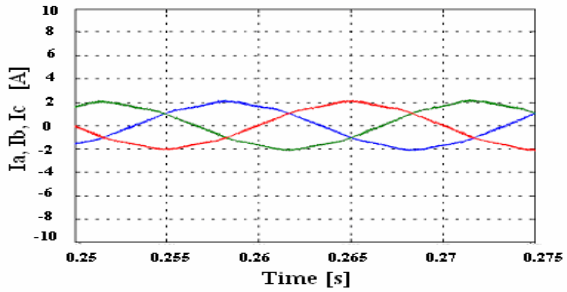

Figure 21. Phase currents from the power network with active filter

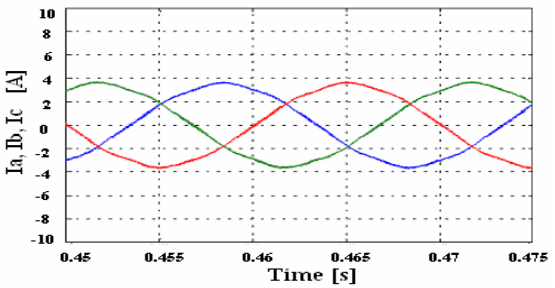

Figure 22. Three-phase currents from the mains supply for dual task

In the following we present the results obtained from simulation for this type of construction.

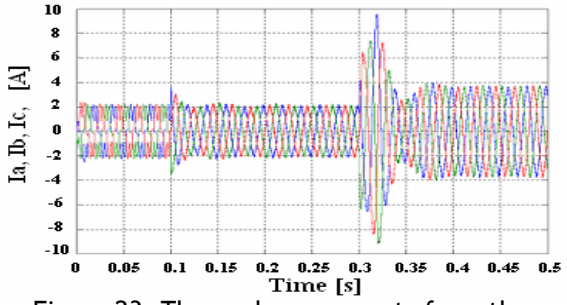

Figure 23. Three-phase currents from the power supply throughout the simulation time

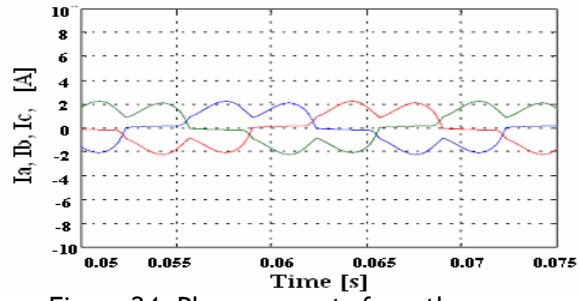

Figure 24. Phase currents from the power network without active filter

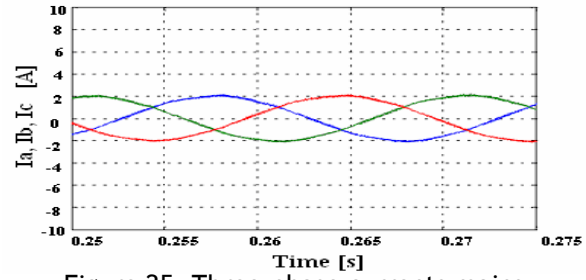

Figure 25. Three-phase currents mains an active filter

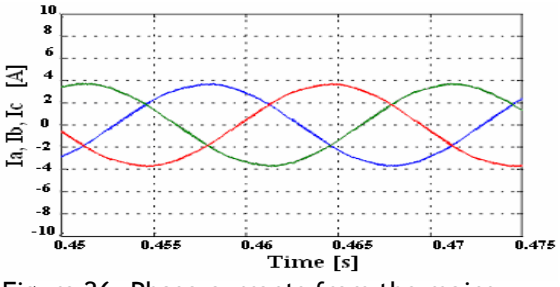

Figure 26. Phase currents from the mains supply for dual task

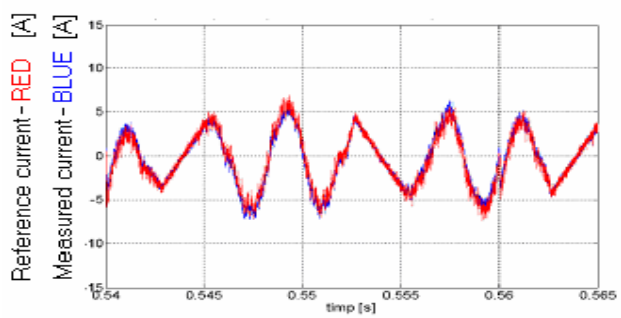

Figure 27. Compensation current produced from the active phase of growth after pregnancy

❖ CONCLUSIONS

This paper presents four schemes using both types of construction, with and without feedback loop, for three-phase voltage sources but balanced nonlinear load (no neutral wire). The first two schemes use a calculation method based on real-time Fourier analysis of the currents on each phase. The other two schemes propose another solution that enables the calculation based on the fundamental harmonic active and reactive power (by averaging the instantaneous value). Simulation of these schemes was done in Matlab-Simulink environment. In all cases observed sharp decrease distorting effect caused by pregnancy. Using sliding mode version requires use of a DSP but need large memory.

❖ REFERENCES

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