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NEW ACHIEVEMENTS IN IMPROVING PQ IN PCCS WITH HIGH DISTORTION AND UNBALANCE BY IMPLEMENTING APFS. PART 2: ACTIVE FILTERING IMPLEMENTATION AND EXPERIMENTAL PERFORMANCES

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Abstract: The analysis of power quality (PQ) in a large enterprise in the point of common coupling (PCC) of the Power Electronics design department shows that, in order to improve the power quality (PQ), three goals must be achieved: the compensation of the distortion power, the compensation of the reactive power and the compensation of the load unbalance. In order to obtain these goals, a four–wire shunt active power filter (SAPF) with split filtering capacitor was designed and built. The SAPF is controlled by implementing the indirect current control method in an original variant. The control algorithm is substantiated and implemented on dSPACE 1103 controlling board. In order to manage the entire system (start, stop and data acquisition), a graphic interface was built and used in experimental evaluation process. The experimental performances obtained for each goal are presented under graphic form and under numeric form of the synthetic indicators. The results show that all the indicators of power quality respect the standards and regulations and prove the validity of the proposed solution.

Keywords: distorting load, unbalanced load, power quality, active power filter

1. INTRODUCTION

The poor power quality (PQ) in the point of common coupling (PCC) of the consumers causes multiple problems with negative effects. Consequently, many scientific papers from literature refer to this topic [4, 20, 23, 31, 33]. Commonly, the big and medium factory have an internal three–phase four–wire distribution network and the loads have a great diversity and many of them are single–phase. Especially, there are three aspects that have negative effects on the power quality: the apparent powers vary rapidly and within extended limits; the currents taken from the PCC are distorted and have a high harmonics content; phase currents are strongly unbalanced [17, 18, 24, 32]. As a result, research has focused on identifying technically feasible solutions that will reduce or even eliminate these effects [7, 8, 15, 16].

In the last 20 years, thanks to developments in power electronics and digital processing techniques, shunt active power filters (SAPF) have become the main means of improving power quality, due to their multiple advantages and reducing manufacturing costs [1, 6, 7, 9, 14, 18, 32, 21, 22, 30]. In three–phase and balanced networks, three–phase three–wire SAPFs can solve successfully the power quality problems [14], [21], but they can't compensate unbalance if it exists. Because of this, solving the problems of power quality in the internal networks of enterprises requires the use of three–phase four–wire SAPFs (4–wire SAPFs). From point of view of the modality of obtaining the connection point of the neutral wire, 4–wire SAPFs have two constructive variants. The first variant uses fourth active branch identical to one corresponding to one phase, and the neutral point is obtained in its middle. This structure is called three–phase four–leg SAPF [1, 6, 13, 18, 22]. In the second variant, the compensation capacitor is divided into two identical capacitors and a three–phase voltage source inverter is used. The neutral wire is connected on the capacitors branch, in their common point [10–12, 32]. This structure is called three–phase three–leg SAPF. Both variants have similar performance, but they are different from complexity of realization point of view. Thus, the three–phase three–leg SAPF variant has a simpler power part and the control part is simpler too. Consequently, this structure has a lower price and it is preferred in many applications under 100 kVA compensated power.

The paper is a continuation of the first Part and it is organized in five main sections: Introduction; Control system; Control algorithm implementation on dSPACE 1103 controlling board; Experimental setup; Experimental results and active filtering performances. In the second section, the SAPF control based on improved method of indirect current control is briefly presented. In the third section, the control implementation on dSPACE 1103 controlling board is presented in detail. In order to manage the entire system (startup, stop and data acquisition), a graphic interface was built and used in the experimental evaluation process. Next, the experimental setup built and connected inside of a large factory is presented. In section four, the performances obtained for each goal are presented under graphic form. The results show that all the indicators of power quality respect the standards and regulations and prove the validity of proposed solution. Finally, few conclusions are drawn.

2. CONTROL SYSTEM

— Cascade two loops control system

The control system of SAPF contains two loops connected in cascade (Figure 1). The control of the DC voltage (on the equivalent capacitor) is done by the main loop (the external one) and the secondary loop is destined of

regulating the current before the PCC. It is specified that the control of the supply current supposes the control on each phase and, consequently, there are three current controllers.
The voltage controller parameters (the imposed voltage, the proportionality constant and the integration time constant) are permanently adapted to the value of the apparent power that is compensated [35–37]. Thus, the voltage controller is of the adaptive PI type.
In order to actualize the DC voltage, its prescribed value is updated at each sampling time by the expression:

$$V_C^* = V_{C\min} + \frac{V_{CN} - V_{C\min}}{\sqrt{S_{FN}}}\sqrt{S_C}\,. \tag{1}$$

For the case of the three–phase three–leg four–wire SAPF, the minimum value of the voltage on the equivalent capacitor (V_{Cmin}) has the expression (double of the maximum phase voltage):

$$V_{C\min} = 2\sqrt{\frac{2}{3}}V_{Le}\,. \tag{2}$$

Because the voltage controller is tuned by the Modulus criterion [25], their parameters are dependent on the compensation capacitor voltage. Consequently, the proportionality constant (K_{pu}) and the integration time constant (T_{iu}), are updated with relation (3):

$$K_{pv} = K_{pvN}\frac{V_C^*}{V_{CN}};\quad T_{iv} = T_{ivN}\frac{V_{CN}}{V_C^*}, \tag{3}$$

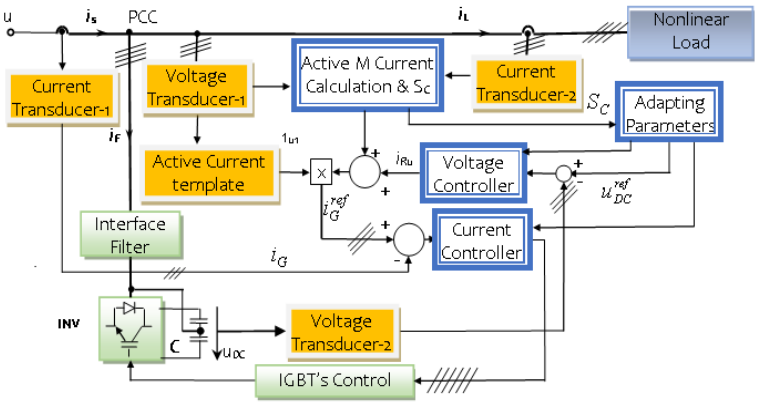

Figure 1. The control system of the three–phase three–leg four–wire SAPF

In (3), K_{puN} and T_{iuN} are the nominal values. Referring to the Figure 1, their values are computed in the "Adapting Parameters".
The current controllers are chosen as hysteresis type, as they are fast and stable. On the other hand, their utilization does the switching frequency to be variable. This disadvantage can be minimized by the proper choosing of the hysteresis band, such that the maximum value of the switching frequency to be limited [3].
The control algorithm needs the following quantities from the power part: the currents on the phases of the power supply; the currents on the phases of the load; the voltages in the PCC; the voltage on the equivalent capacitor. All of them are obtained from the corresponding transducers.

— Current Control

For the current control on the AC side, an improved variant of the indirect current control method (ICC) published by authors [27] was adopted. Thus, the current imposed to the current controllers contains two components (Figure 1): the equivalent current corresponding to a balanced active load (i_{La}^*) and the loss current whose amplitude is obtained from voltage controller (i_{loss}^*):

$$i_g^* = i_{La}^* + i_{loss}^*\,. \tag{4}$$

The amplitude of the equivalent active current is computed from the total active power of the load (P_L), by summing the phase active powers:

$$P_L = P_{L1} + P_{L2} + P_{L3} = \frac{1}{T}\sum_{k=1}^{3}\int_{t-T}^{t} v_{Lk} i_{Lk}\,dt\,. \tag{5}$$

It was neglected the neutral voltage because the power transformer has the power much bigger than the load. In fact, the experimental data showed that the neutral voltage is very close to zero. This means that the active power received by the load on the neutral wire is very low and can be neglected.
The equivalent value of the RMS phase voltage is calculated with the general expression [5], [19]:

$$V_{Le} = \sqrt{\frac{1}{3}\left(V_{L1}^2 + V_{L2}^2 + V_{L3}^2\right)}\,. \tag{6}$$

Thus, the amplitude of the active current equivalent to the balanced load is obtained in the block "Active M Current Calculation & SC" (Figure 1) as:

$$I_{vLe} = \sqrt{2}\frac{P_L}{3V_{Le}}\,. \tag{7}$$

The amplitude of the prescribed current is calculated as the sum of the amplitude of equivalent active current given by (7) and the amplitude of the losses current obtained from voltage controller output. Next, the prescribed instantaneous current is obtaining by multiplying its amplitude with the sinusoidal signals of unit amplitude and having the same phase as the fundamental phase voltages that are obtained from the "Active Current template" block (Figure 1).

3. CONTROL ALGORITHM IMPLEMENTATION

The control algorithm was implemented on the dSPACE DS1103 prototyping board. As software support, the control implementation uses the Simulink model/subsystem (Figure 2) that contains three main parts.

≡The capacitor voltage control loop, which receives three signals:

- ✓ The imposed voltage on the compensating capacitor;
- ✓ The parameters of controller (the proportionality constant and integration time constant).

≡The AC current control loop.

≡Auxiliary blocks:

- ✓ The initialization sequence of power section [2];
- ✓ The protection block, which validates the gating signals for the power transistors, only when the closed loop control system is valid [25], [29].

The imposed voltage of voltage controller, as well as its parameters, are received from the adaptation section which is outside of the control subsystem [26].

The complete control algorithm is obtained after connecting the Simulink model with input–output ports of DS1103 prototyping board (Figure 3).

The gain blocks (in yellow) are necessary in order to adapt the level of transducers signals to the dSPACE board rated inputs (±10 V). The gains used are: 1000 for AC side voltage transducers; 1500 for compensating capacitor voltage transducer; 150 for current transducers.

The control algorithm input connections are detailed in Table 1. The gate signals for the IGBTs come from the outputs of hysteresis current controllers and are send by six Digital Output.

The entire algorithm is controlled by two auxiliary signals: vINC that validates the operation of voltage controller and the gates control signals vCOMP that validates the compensation in accordance with the control algorithm.

In accordance with the model complexity, the solving method was ode 1 and the sample time was 20 µs.

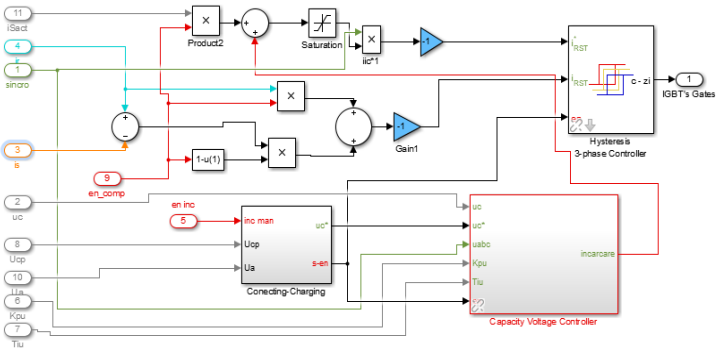

Figure 2. The active filter control subsystem

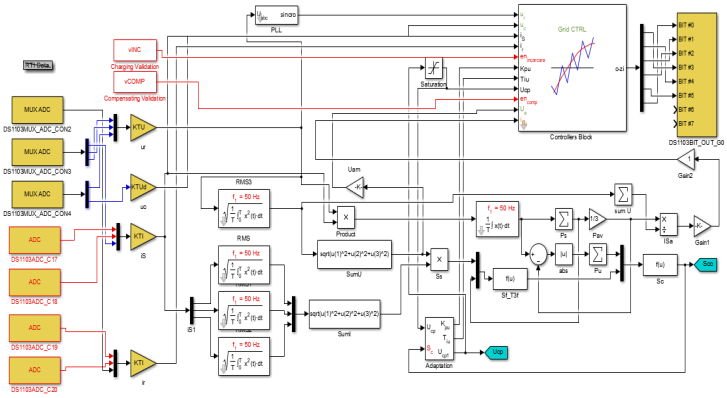

Figure 3. The experimental active filter control system

Table 1. The control algorithm input connections.

Input port	Signal description
Mux_ADC_CON3_2	Power grid voltage (u_a)
Mux_ADC_CON3_3	Power grid voltage (u_b)
Mux_ADC_CON4_1	Power grid voltage (u_c)
Mux_ADC_CON4–2	Compensating capacitor voltage (u_{dc})
ADCH17	Load current (phase a)
ADCH18	Load current (phase b)
Mux_ADC_CON3_1	Load current (phase c)
ADCH19	Power grid current (phase a)
ADCH20	Power grid current (phase b)
Mux_ADC_CON2	Power grid current (phase c)

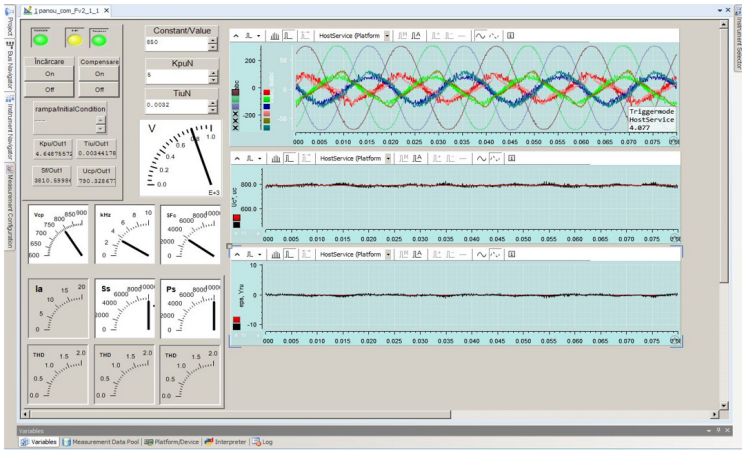

Figure 4. The experimental active power filter control panel

In order to manage the experimental tests, a virtual control panel under specific software ControlDesk NG was build (Figure 4) [28], [34] –37]. It contains all the instruments needed to initialize the control algorithm, start–stop of the experimental setup and saving the shape or numeric values of the quantities of interest.

It also contains:

- A Start/Stop button that validates the beginning of the compensating capacitor charging sequence and assigns a constant value to the output of the Constant block;
- A button destined to the manual validation of the compensation process;
- Several virtual oscilloscopes needed for the performances determination and the qualitative analysis, after completing the experiments;
- Several numeric input instruments for: the initial imposed start–up voltage on the compensating capacitor; nominal values of the proportional constant and integration time constant of the voltage controller; compensating capacitor steady–state imposed value (if it is necessary).

4. EXPERIMENTAL SETUP

In order to significantly improve the power quality in PCC, the grid must provide only active power distributed equally on each phase. This supposes that the following powers of the load must be compensated: the distortion power; the reactive power and the unbalance power. For this, a four–wire three–leg shunt active power filter was designed and built. The compensation capacitance was equally divided, for connecting with the transformer neutral point.

Table 2. The main parameters of the system.

Items	Values
Supply Transformer	Connection D/y0, 6/0.4 kV, S_N=1000 kVA
SAPF transistors	IGBTs, SKM100GB12T4, V_{CE}=1200 V, I_C=100 A
Interface filter	L_{fi} = 4 mH
DC–capacitor	Cc=1200 μF
Voltage controller	PI type, K_{puN}=0.2; T_{iuN}=40 ms
Hysteresis band	0.5 A

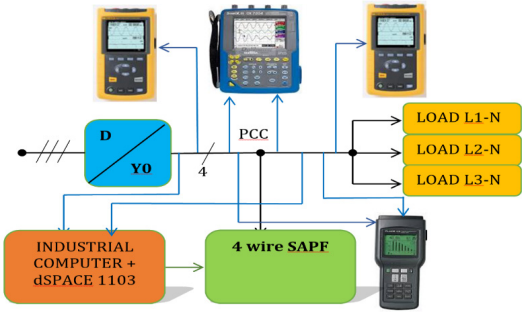

Figure 5. The structure of the experimental setup

Figure 6. Picture of the experimental setup

In Table 2, the main parameters of the power part are shown.

The experimental structure (Figure 5) includes:

1. The active power filter developed as a prototype;
2. The dSPACE 1103 prototyping board placed into an industrial computer;
3. Two Fluke 435 power quality analyzers connected upstream and downstream of the PCC respectively;
4. A METRIX OX 7042 oscilloscope;
5. A Fluke 41b analyzer.

A picture of the experimental setup is given in Figure 6.

5. EXPERIMENTAL RESULTS AND ACTIVE FILTERING PERFORMACES

In order to collect the data necessary to determine the performance of the active filtering system, SAPF was connected to the PCC and the capacity charging sequence was started. Next, the control algorithm was validated and the waveforms of currents and voltages were recorded. The Fluke 41b analyzer was used for recording the main indicators of power quality. Also, during 65 minutes, the Fluke 435 analyzers recorded all the indicators of the power quality to the load side and to the grid side.

The multiple registrations were intended to verify the effectiveness of the proposed solution in several ways. In order to analyze the results presented in the different figures, it must be notified that they do not correspond to the same time interval. This is a consequence of limited number of measuring devices input channels, but it does not affect the intended purpose.

— Compensation of the distortion power

The distorted waveforms of the load currents and the sinusoidal waveforms of the grid currents show that the distortion power is compensated (Figure 7).

The load currents have the harmonic distortion factor different on the three phases, respectively THD is of (9.5 – 42.9) % (Figures 8–10). The THD of the grid currents is reduced under 8 % on each phase, after harmonic compensation (Figure 11).

The values recorded by Fluke 435 analyzers, at the same time moments, show that the filtering efficiency on each phase, calculated as the ratio of THD factors before and after compensation, are: on phase A, between 6 % and 9 %; on phase B, between 4 % and 10 %; on phase C, between 2 % and 6 % (Figure 12).

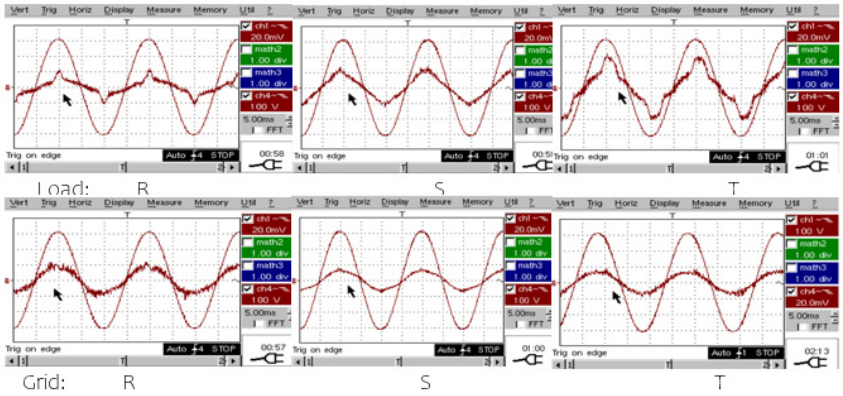

Figure 7. The currents on the phases of the load and of the grid.

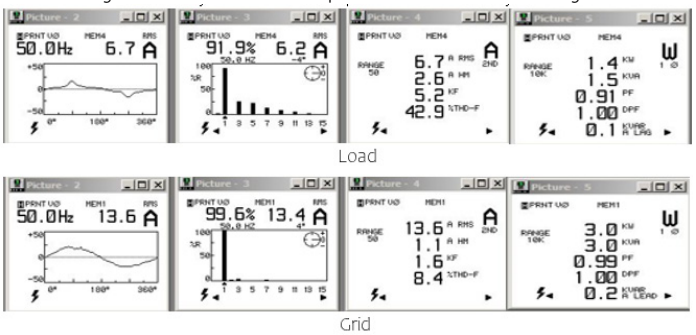

Figure 8. The shape of the current and the main power quality indicators on phase R of the load and of the grid (Fluke 41B).

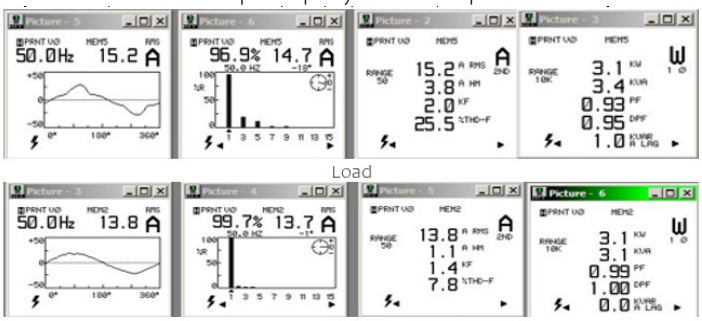

Figure 9. The shape of the current and the main power quality indicators on the phase S of the load and of the grid (Fluke 41B).

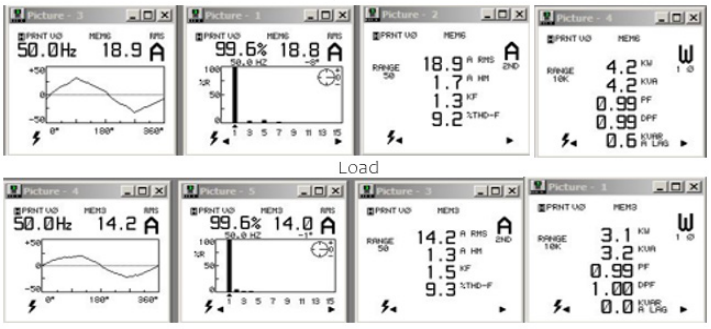

Figure 10. The shape of the current and the main power quality indicators on the phase T of the load and of the grid (Fluke 41B).

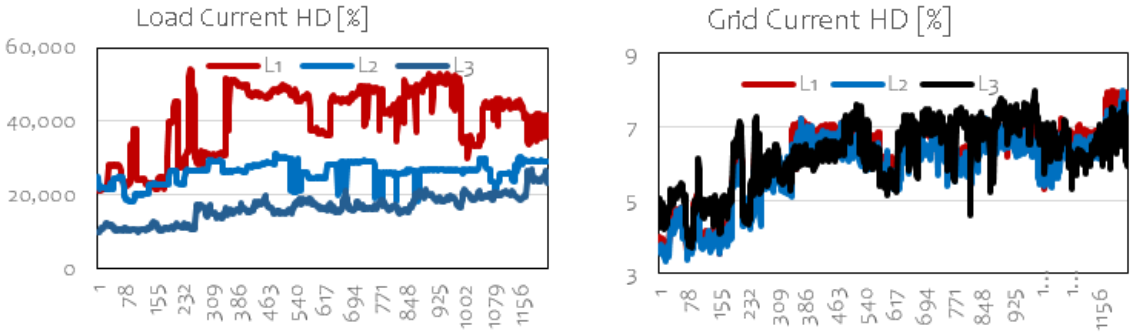

Figure 11. Harmonic distortion factor of the currents on the load side and on the grid side during recording (Fluke 435).

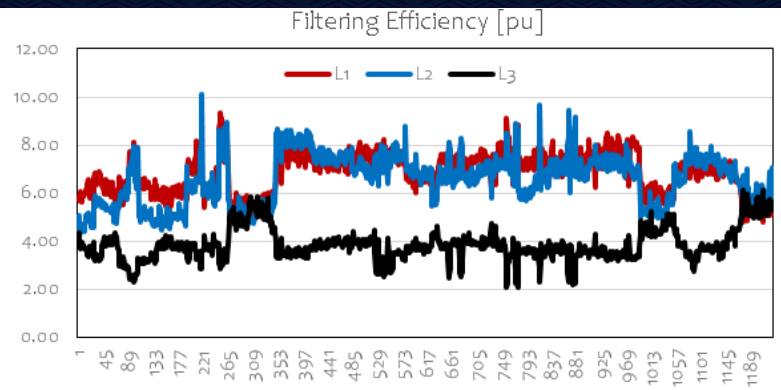

Figure 12. The filtering efficiency during recording.

— Reactive Power Compensation

The waveforms of the phase voltages and currents at the grid side (Figure 7) show that the reactive power is very well compensated because their phases coincide. Also, it can be seen that the power factors on each phase are practically unitary (Figure 8–10). The same aspects are proved by the time evolution of the total power factor during the recordings, upstream and downstream of the PCC. This evolution shows the very good performance, both in compensating the distortion power and in compensating the reactive power (Figure 13). Thus, the power factor on the phases at the load side (downstream of the PCC), for most of the interval, has values between 0.83 and 0.97, but after compensation, up–stream of the PCC, the values are 0.94–0.98.

— Unbalance Compensation

In order to characterize the load unbalance, the unbalance index was used. It is defined as the deviation of the RMS value of the phase current from the average value of all phase currents (I_{av}).

$$\varepsilon_{unLABC} = \frac{I_{A,B,C} - I_{av}}{I_{av}}. \tag{8}$$

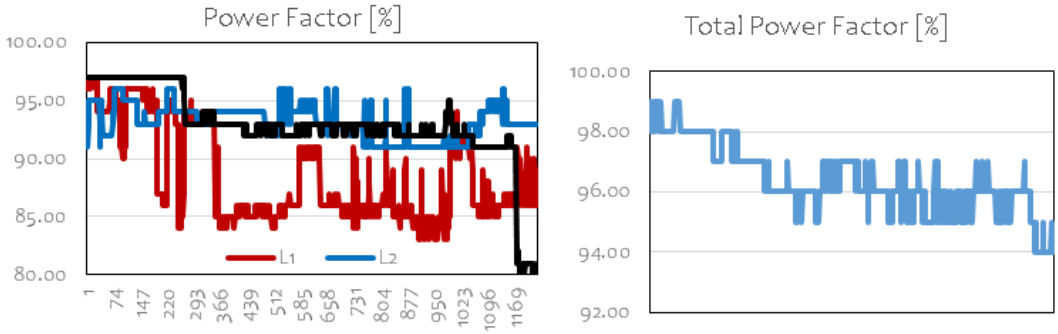

Figure 13. Total power factor on the load side and on the grid side during recording (Fluke 435)

$$I_{av} = \frac{I_A + I_B + I_C}{3}. \tag{9}$$

Figure 14 shows the evolution of unbalance index during recordings. It can see that the load current unbalance change quickly between –50 % and 50 %, because the phase currents (RMS values) are much different and they change quickly (Figure 15). Contrary, the grid currents have the RMS values slightly different due to registration error (±1 A) (Figure 15).

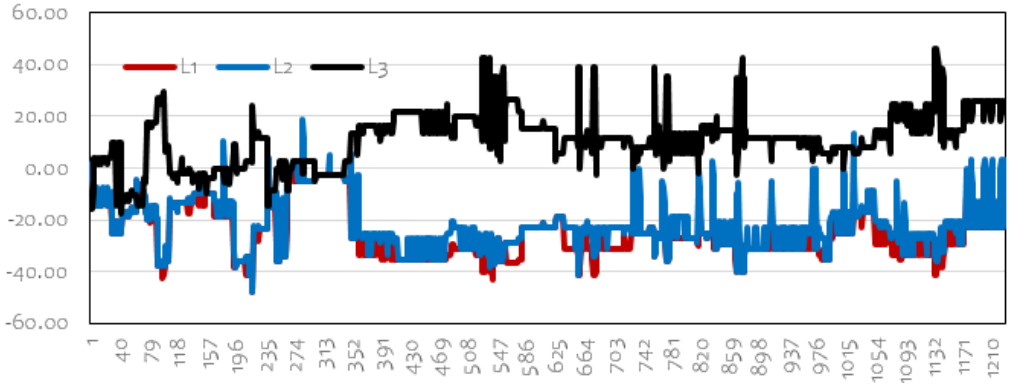

Figure 14. The unbalance index on the load side during recording (Fluke 435).

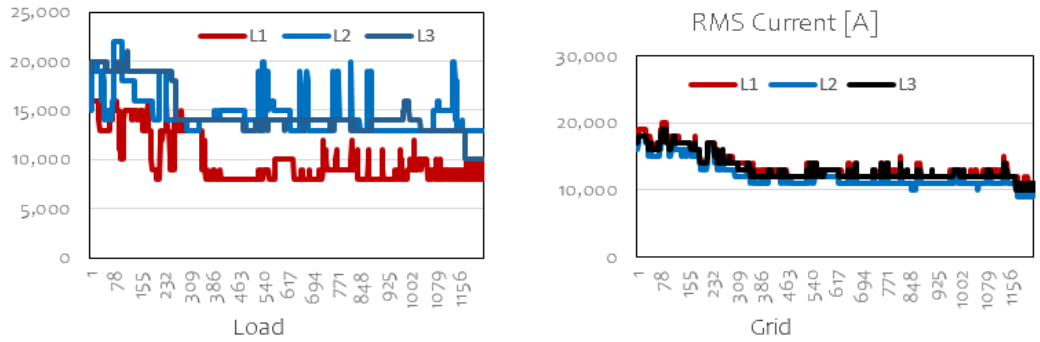

Figure 15. The currents on the load side and on the grid side during recording (Fluke 435).

6. CONCLUSIONS

— The measurements done in the PCC of the Industrial Electronic Department of a large enterprise revealed that there are major problems with energy quality. Thus, to solve this problem, it was chosen the active filtering solution using a four–wire three–leg SAPF with divided compensation capacitor, that was designed and built as a prototype.

— An advanced control algorithm was used, which is based on an improved indirect current control and an adaptive PI voltage controller.

— The hardware part for the control algorithm implementation was the DSP prototyping system dSPACE 1103.

— In order to collect the experimental data, a dedicated graphical interface was built and four devices (the two–channel METRIX OX 7042 oscilloscope, two Fluke 435 Analyzers and a Fluke 41B Analyzer) were used.

— The measurements were performed on an time interval more that 1.5 hours corresponding to the maxim load and the power quality parameters were recorded simultaneously, upstream and downstream of the SAPF connection point.

— A part of recorded data was processed and together with other part (waveforms or numerical values) highlight that the proposed solution determines very good performance, respectively:

- ✓ The harmonic distortion factors of the phase grid currents are within the imposed limits by norms;
- ✓ The obtained filtering efficiency has high values (maximum value is over 10);
- ✓ As a consequence of compensating the distortion power and the reactive power, the power factor at the grid side become almost unitary;
- ✓ Although the load current is high unbalanced, the grid currents are practically equal because the unbalance active power is also compensated.

— In the considered case study, in order to solve the problems of power quality, the proposed active filtering system, consisting of a three–phase three–wire SAPF with divided capacitor and improved and adaptive control algorithm, is an appropriate solution.

Note: This paper was presented at XXth National Conference on Electric Drives – CNAE 2021/2022, organized by the Romanian Electric Drive Association and the Faculty of Electrotechnics and Electroenergetics –University Politechnica Timisoara, in Timisoara (ROMANIA), between May 12–14, 2022 (initially scheduled for October 14–16, 2021).

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